

MASTER DRAWING LIST

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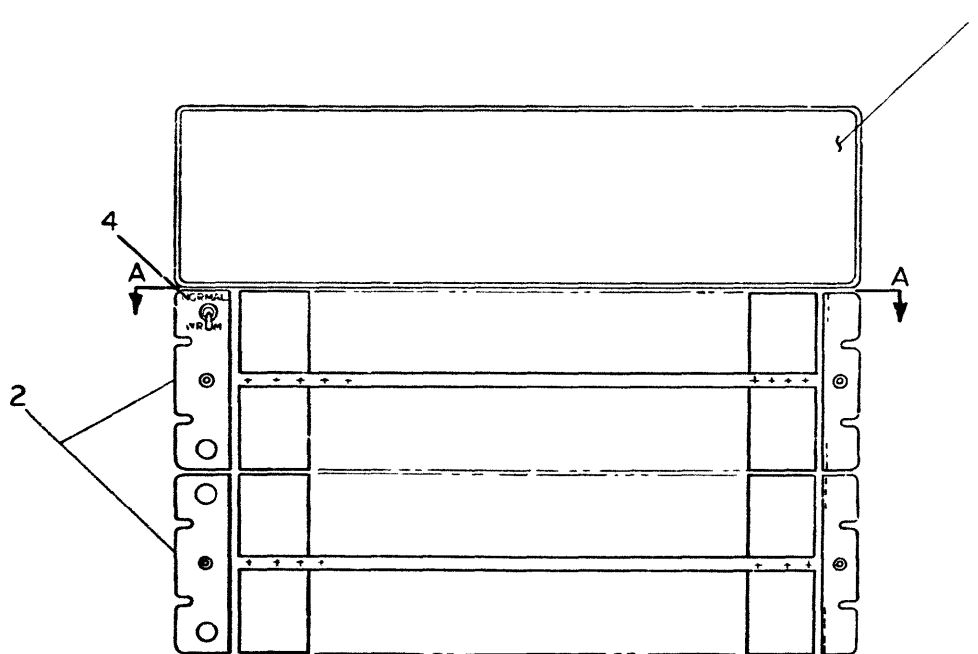
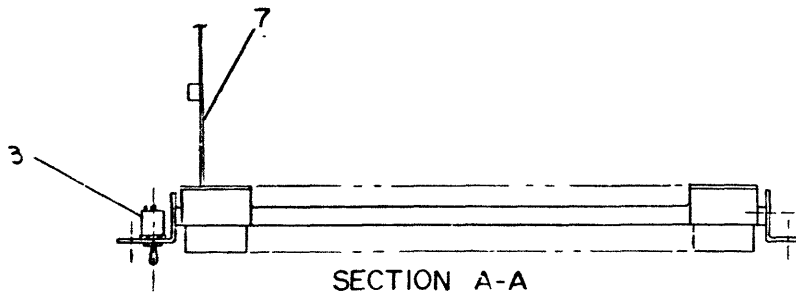
DWG. NO.	REV. LET.	NO. OF SHEETS	TITLE
D-UA-TC08-0-0	E	1	DECTAPE CONTROL
A-PL-TC08-0-0	E	1	DECTAPE CONTROL
D-BS-TC08-0-1	F	1	I/O CONTROL
D-BS-TC08-0-2	F	1	STATUS "A"
D-BS-TC08-0-3	H	1	TP GEN
D-BS-TC08-0-4	F	1	FLAGS
D-BS-TC08-0-5	C	1	CONTROL
D-BS-TC08-0-6	E	1	ERRORS
D-BS-TC08-0-7	B	1	MARK TRACK DECODE
D-BS-TC08-0-8	A	1	DTB/WB
D-BS-TC08-0-9	B	1	LPB
D-BS-TC08-0-10	B	1	I/O BUS INVTs/IND DVRS
D-BS-TC08-0-11	C	1	I/O BUS DRIVE/RECEIVE
D-TC-TC08-0-12	B	1	I/O BUS CONNECTORS
K-(MI)-TC08-0-13 (PL)	F	2	MODULE UTILIZATION LIST
K-WL-TC08-0-14	T	1	WIRE LIST TC08
D-AD-7006394-0-0	C	1	WIRED ASS'Y TC08
A-PL-7006394-0-0	C	1	WIRED ASS'Y TC08
A-AT-7006394-0	U	1	AWT REVISION STATUS
D-DI-TC08-0-15	F	1	DECTAPE CONTROL
A-SP-TC08-0-16	B	1	CHECK-OUT PROCEDURE
D-TD-TC08-0-17		1	TC08 TIMING
D-IC-TC08-0-18	D	2	AC POWER WIRING
D-IC-TC08-0-19	B	1	DC POWER WIRING
D-TC-TC08-0-20		1	CABLE CONFIGURATION
D-AR-TC08-0-21	C	1	CABINET LAYOUT
A-SP-TC08-0-22		2	ACCEPTANCE PROCEDURE
A-SP-TC08-0-23		49	ENGINEERING SPECS
D-AR-TC08-0-24		1	DECTAPE CAB LAYOUT
A-BI-TC08-0-25	A	1	ACCESSORY LIST

REVISIONS				DRN. G. GIANOULOS	DATE 6/13/89	 DIGITAL EQUIPMENT CORPORATION <small>MAYNARD, MASSACHUSETTS</small>		
REV.	DATE	CHG. NO.	APP'D.	CHK'D R. COOK	DATE			
AF	1-73	00027	LN	ENG. D. LAZIUKA	DATE	TITLE DECTAPE CONTROL 60 HZ		
AH	3-75	00028	LN	PROJ. ENG. D. LAZIUKA	DATE			
AJ	DEC-76	00029	LN	PROD. F. LASKEY	DATE			
				FIRST USED ON				
				SCALE	A ML	SIZE CODE	NUMBER	REV.
				SHEET 1 OF 1	DIST.		TC08-0	AJ

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LEGEND	
NUMBER	VARIATION
TCØB-Ø	60 HZ
TCØB-A	50 HZ

WIRE TABLE				
TEW NO	DESCRIPTION	CONNECTIONS		REMARKS
NO	AWG	COLOR	FROM	TO
5	24	BLACK	SW-2	B3,C2
6	24	YEL	SN-3	B3,BV



REV	CHANGE NO	DATE	BY	APP
1	TCØB-ØØØØ	11-71	D LARINA	
2	TCØB-A	11-71	R. J. ...	
3	TCØB-ØØØØ	11-71	NARHI	
4	TCØB-ØØØØ	11-71	NARHI	
5	TCØB-ØØØØ	11-71	NARHI	
6	TCØB-ØØØØ	11-71	NARHI	
7	TCØB-ØØØØ	11-71	NARHI	

FIRST USED ON OPTION / MODEL
TCØB

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS FRACTIONS ANGLES
± .005 ± .004 ± .002
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH

QTY	DESCRIPTION	PART NO.	ITEM NO.
PARTS LIST			
DRW	DATE	digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS	
CHK	DATE	TITLE	
ENG	DATE	DECTAPE CONTROL.	
PROJ. ENG.	DATE	NEXT HIGHER ASSY	
PROD.	DATE	A-MLTCØB-Ø-Ø	
SCALE NONE		SCALE CODE	NUMBER
SHEET 1 OF 1		DIST	REV
		DIST	F

PART NO. TCØB-Ø-Ø
 REV. E
 DRAWN BY: [Signature]
 CHECKED BY: [Signature]

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS
PARTS LIST

QUANTITY / VARIATION

MADE BY G. MARI: I	CHECKED P. COOK	SECTION
DATE 6/23/69	DATE 7/24/69	ISSUED SECT.
ENG	PROD	
DATE	DATE	

ITEM NO	DWG NO. / PART NO.	DESCRIPTION
1	D-A-7006331-5-0	INDICATOR PANEL ASSY (TC08)
2	D-AD-7006334-0-0	WIPE ASSY (TC08)
3	1202279	WITCH TOGGLE
4	A-DC-5308493-0-0	D-CABLE (TC08)
5	9107450-44	WIPE = 24 AWG TRD TEF INS BLK
6	9107450-44	WIPE = 24 WG TRD TEF INS YEL
7	D-UA-BC08C-0-0	CABLE, DUAL NYLAR M003-(2) #031
*	D-UA-854-C-0	POWER CONTROL 854C
*	D-UA-854-B-0	POWER CONTROL 854B
*	D-UA-783-0-0	783 POWER SUPPLY
*	D-UA-783A-0-0	POWER SUPPLY TYPE 783A
*	E-AJ-7005474-0-0	ANAL SS
*	D-AD-7005909-0-0	AC DIST PANEL
*	7005128	POWER COND 25'
*	1209340-1	Mat-N-LOC CONN
*	1209378-1	PIN, CONTACT
8	7C06223-0	INTERCONNECTING CABLE
*	D-UA-H721-0-0	POWER SUPPLY H721
*	D-UA-H721-A-0	POWER SUPPLY H721A
*	NOT SHOWN ON ASSY	

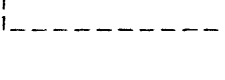
TC08-0-01Z	TC08-A-01Z																			
1	1																			
1	1																			
1	1																			
1	1																			
1	1																			
A/BA/B																				
A/BA/B																				
5	5																			
1																				
1																				
7																				
3																				
1	1																			
1	1																			
1																				
1	1																			
8	8																			
1	1																			
1	1																			

TITLE DECTAPE CONTROL	ASSY NO D-UA-TC08-0-0	SIZE A	CODE PL	NUMBER TC08-0-0	REV E	ECO NO. TC08-00024
	SHEET 1 OF 1	DIST G				

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NOTE:
TC084 ONLY

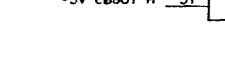
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- I/O BMB 04 (1) L R1
- I/O BMB 05 (1) L S1
- I/O BMB 06 (1) L U1
- I/O BMB 07 (1) L H2
- I/O BMB 08 (0) L T2



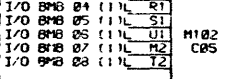
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- I/O BMB 04 (1) H E2
- I/O BMB 05 (1) H F2
- I/O BMB 06 (1) H H2
- I/O BMB 07 (1) H J2
- I/O BMB 08 (0) H K2
- +3V C08U1 H L2
- +3V C08U1 H N2



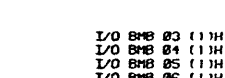
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- +3V C08U1 H J1



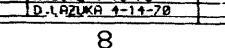
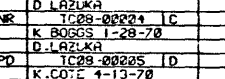
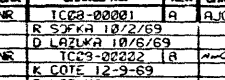
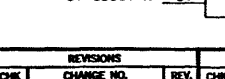
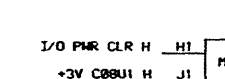
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- I/O BMB 04 (1) L R1
- I/O BMB 05 (1) L S1
- I/O BMB 06 (1) L U1
- I/O BMB 07 (1) L H2
- I/O BMB 08 (1) L T2



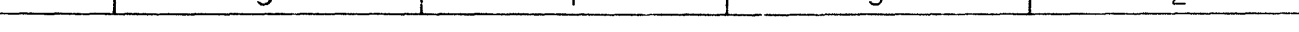
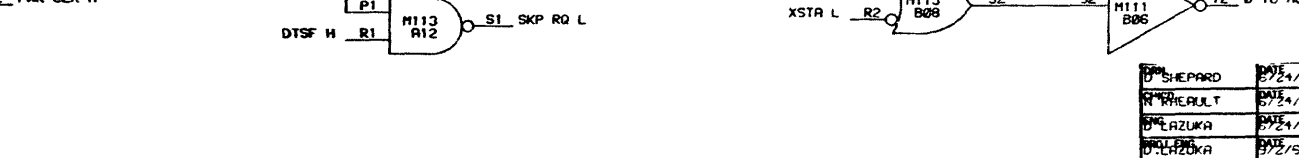
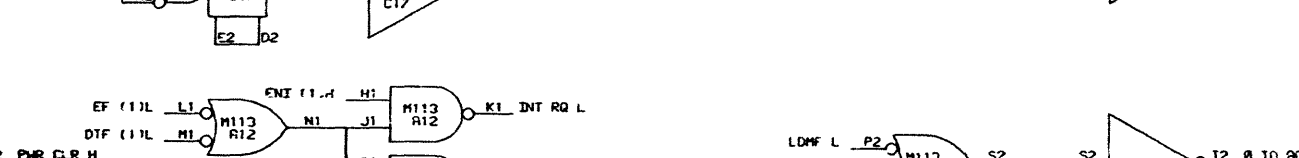
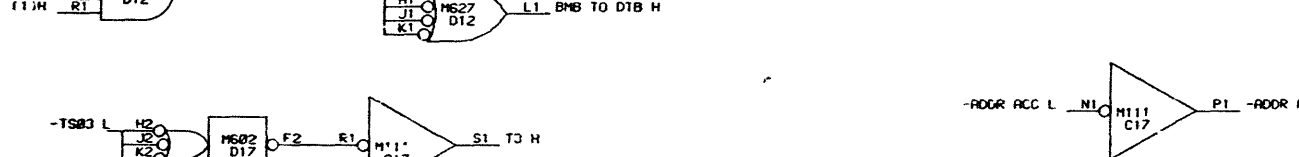
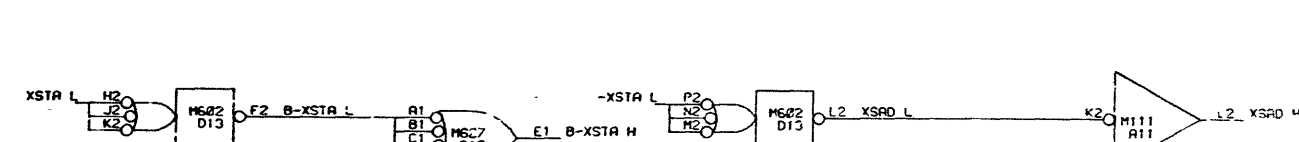
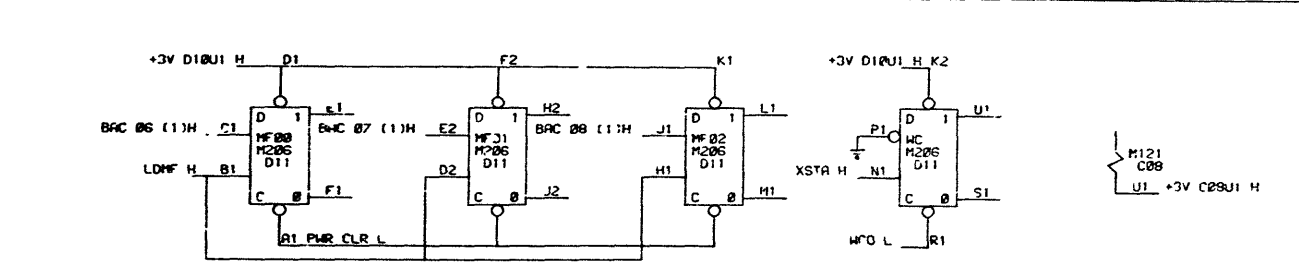
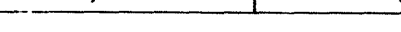
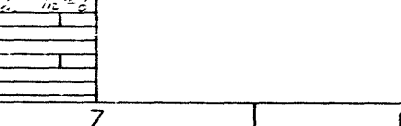
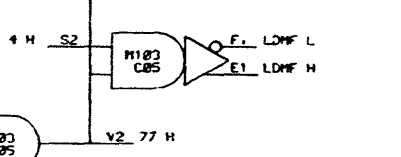
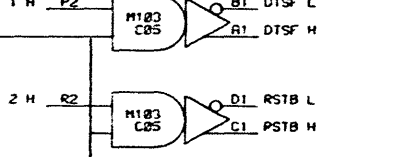
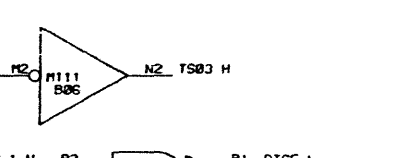
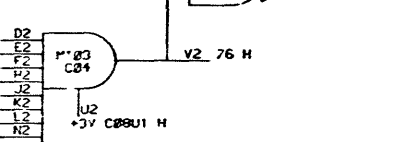
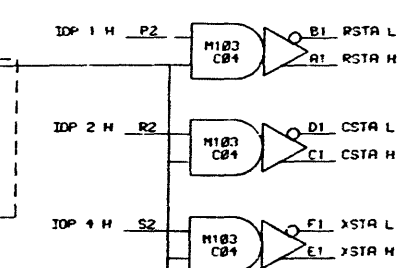
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- I/O BMB 04 (1) H E2
- I/O BMB 05 (1) H F2
- I/O BMB 06 (1) H H2
- I/O BMB 07 (1) H J2
- I/O BMB 08 (1) H K2
- +3V C08U1 H L2
- +3V C08U1 H N2



- I/O PWR CLR H H1
- +3V C08U1 H J1

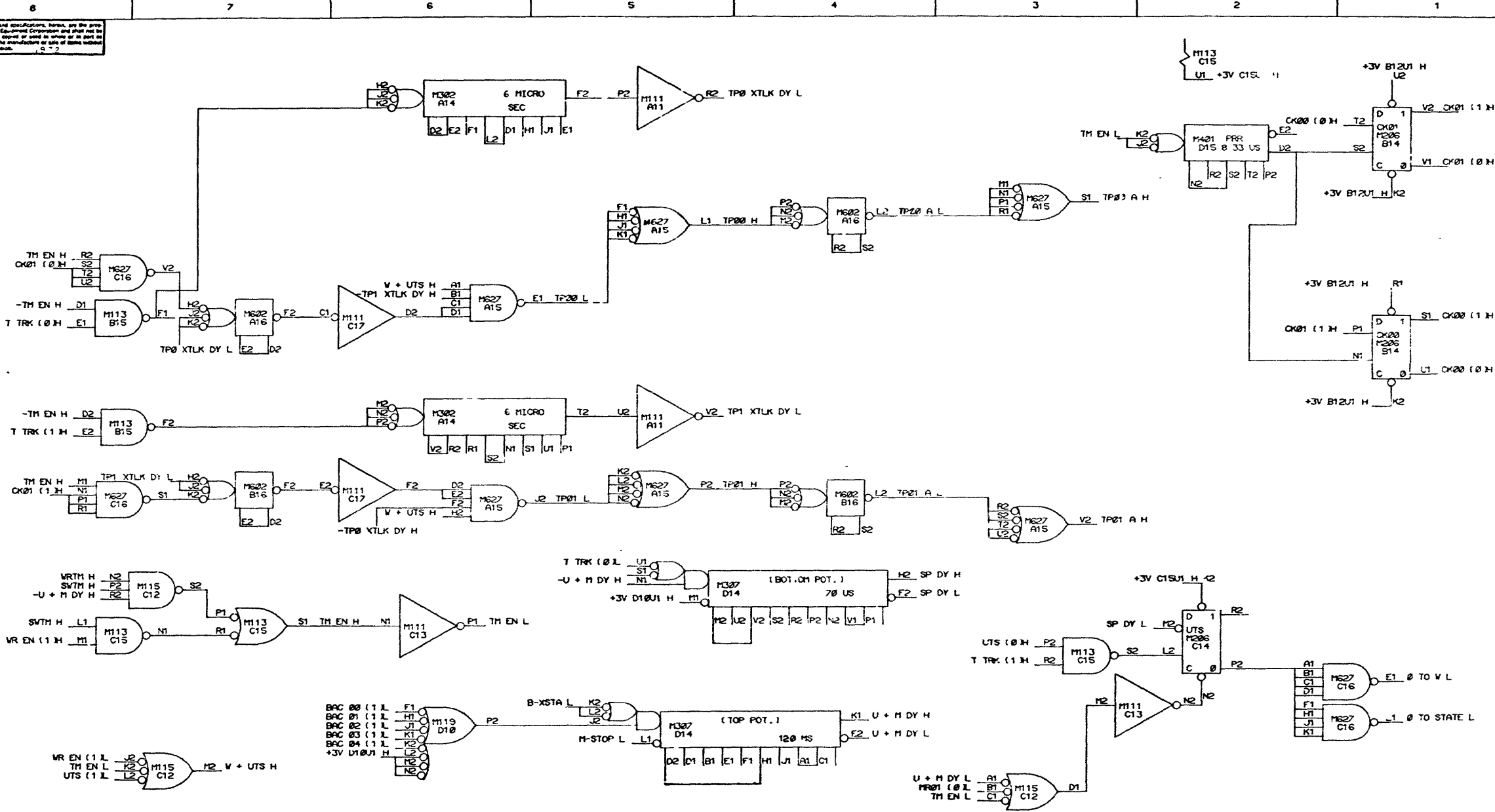


REVISIONS			REVISIONS		
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NR	TC08-00001	A	AJC	TC08-00205	F
R	SOPKA 10/2/69		P	WASH-DIS-524 4-24-70	
D	LAZUKA 10/6/69		D	LAZUKA 4-24-70	
NR	TC08-00202	A	NR	TC08-00212	F
K	COTE 12-9-69				
D	LAZUKA				
NR	TC08-00004	C			
K	BOUGGS 1-28-70				
D	LAZUKA				
PD	TC08-00205	D			
K	COTE 4-13-70				
D	LAZUKA 4-14-70				



DATE	3/24/69	digital EQUIPMENT CORPORATION MAYFIELD MASSACHUSETTS
BY	W. SHEPARD	
DATE	3/24/69	TITLE
BY	D. LAZUKA	
DATE	3/24/69	I/O CONTROL
BY	D. LAZUKA	
DATE	3/24/69	FIRST USED ON
BY	P. LASKEY	
TC08		SCALE
TC08		SIZE CODE
D 55	TC08-0-1	NUMBER
		REV.
		F
SHEET	1	OF
		DIST

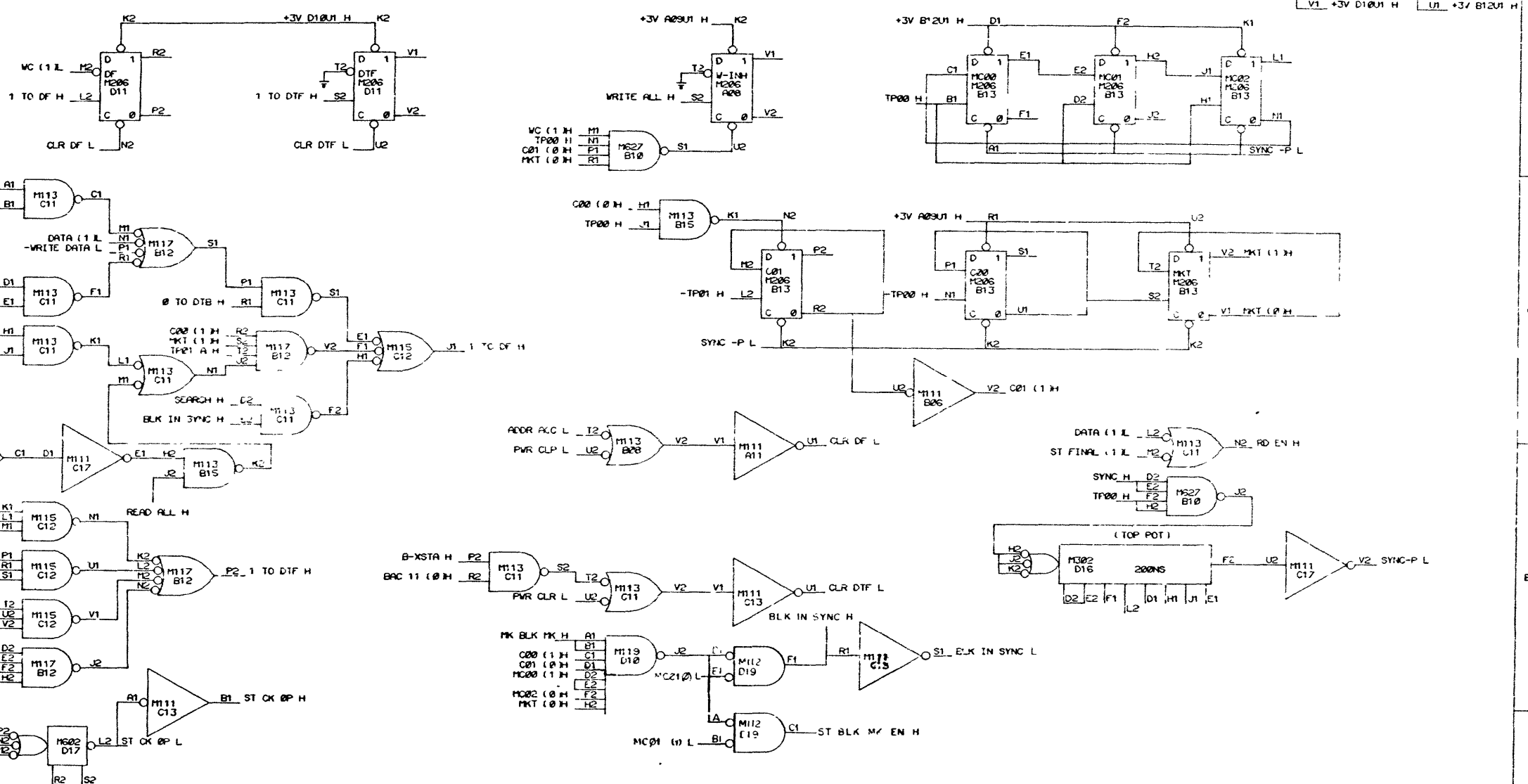
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REVISIONS			REVISIONS		
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NR	TC08-02201	A		TC08-00020	F
	R SCFKA 12-2-63				
	D LAZUKA 12-6-69				
	TC08-22205	B		TC08-00022	F
	A WASHINGTON				
	D LAZUKA 4-14-70				
HWC	TC08-22205	C		TC08-00026	H
	A WASHINGTON 4-24-70				
	D LAZUKA 4-24-70				
GH	TC08-02012	D			
	ADS				
	D LAZUKA 7/7/71				

DRN D. SHEPARD	DATE 6/24/69		EQUIPMENT CORPORATION MILFORD, MASSACHUSETTS
CHKD N. REAULT	DATE 6/24/69		
ENG D. LAZUKA	DATE 6/24/69	TITLE TP GEN	
PROJ ENG D. LAZUKA	DATE 9/2/65		
DRK F. LASKEY	DATE 9/2/65		
FIRST USED ON TC08		SIZE CODE D ES	NUMBER TC08-0-3
SCALE	1 OF 1		REV. 11
SHEET	1 OF 1	DIST	

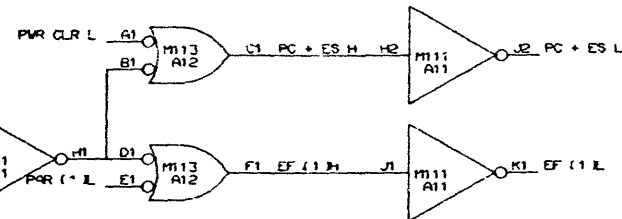
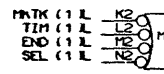
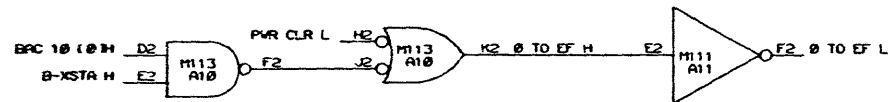
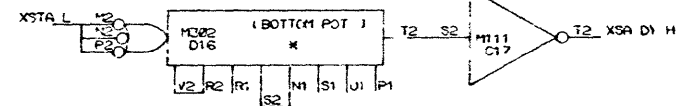
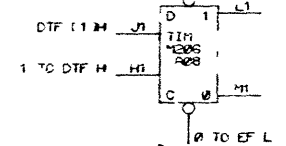
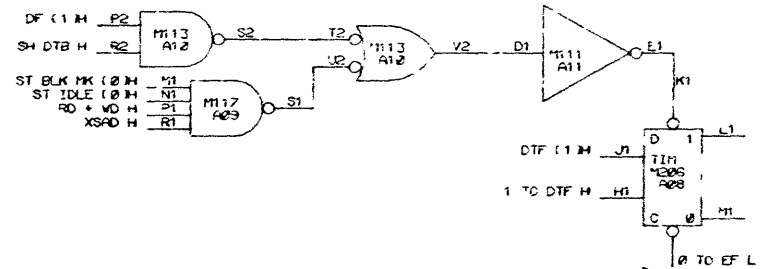
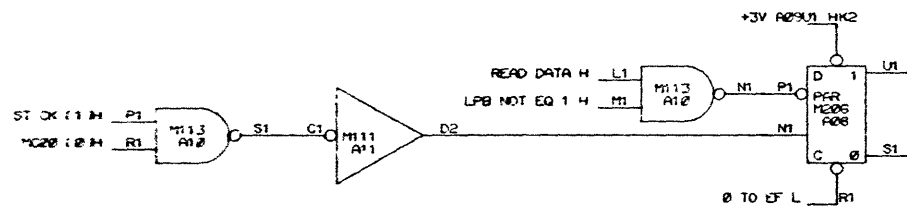
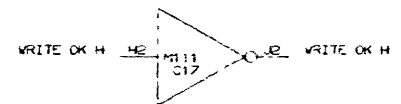
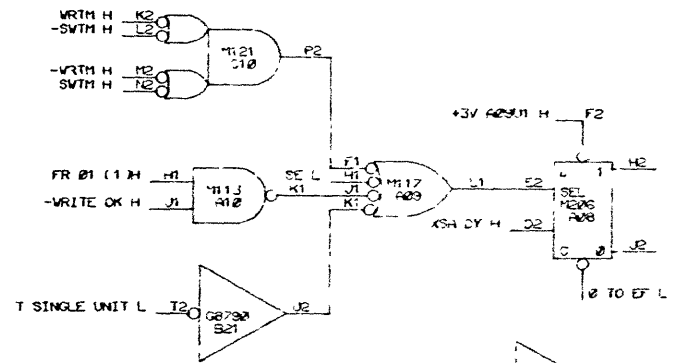
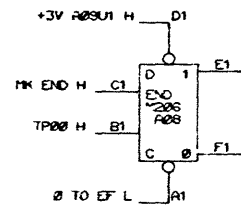
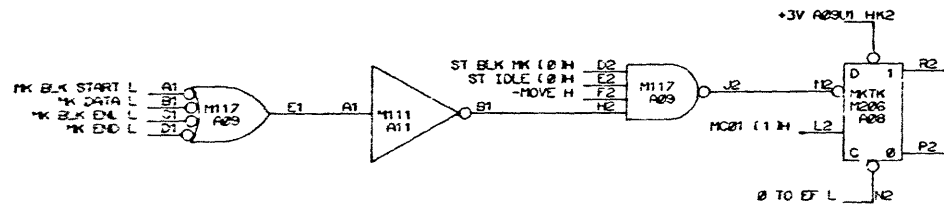
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REVISIONS			REVISIONS		
CHK	CHANGE NO.	REV.	CHK	CHANGE NO.	REV.
NR	TC08-00201	A		TC08-00203	E
	R. SOYKA 10-2-63				
	D. LAZUKA 10-6-63			KIPK	
PD	TC08-00205	B			
	A. WASHINGTON 4-8-70				
	D. LAZUKA 4-14-72				
CH	TC08-00208	C			
	I. PETERS 7/9/70				
	D. LAZUKA 7/9/70				
	TC08-00218	D			

DESIGNED BY	D. SHEPARD	DATE	6/24/63	EQUIPMENT CORPORATION
DRAWN BY	N. R. CAULT	DATE	6/24/63	
CHECKED BY	D. LAZUKA	DATE	6/24/63	TITLE
DESIGNED BY	D. LAZUKA	DATE	6/24/63	FLAGS
DESIGNED BY	E. LASKEY	DATE	9/2/63	
FIRST USED ON	TC08	SCALE	D. B. S.	NUMBER
		SHEET	1 OF 1	REV.
		DIST	TC08-0-1	E

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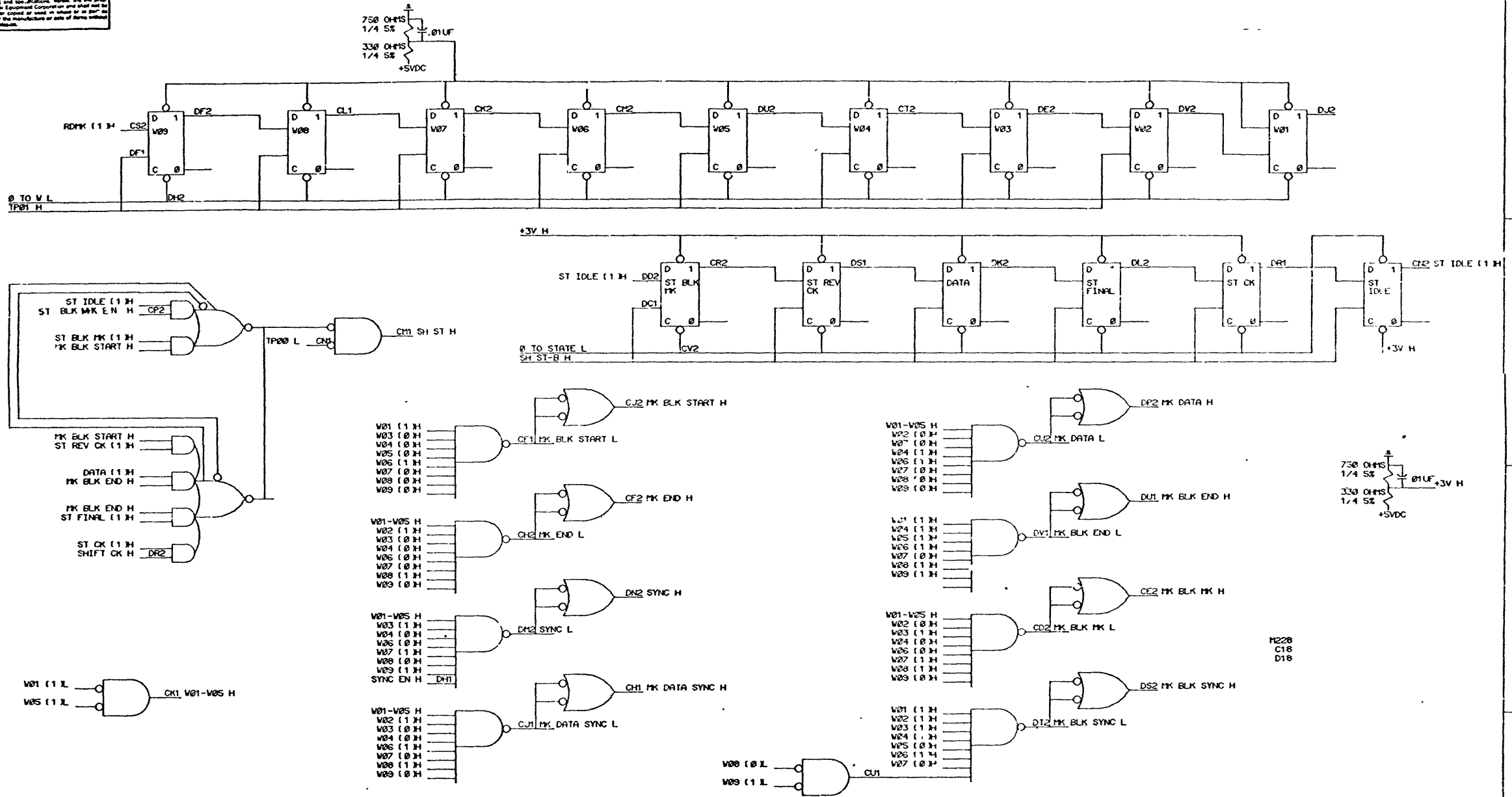


* ALL SYSTEMS 3 MICRO SEC

REVISIONS			REVISIONS		
CHK	CHANGE NO	REV	CHK	CHANGE NO	REV
NR	TC08-00001	3		TC08-00021	E
R	OP73 10-2-53				
Q	LAZ KR 10-8-53				
PD	TC08-00005	B			
A	WASH ASTON 4-8-70				
Q	TC08-00014	10			
K	WALSH 5-7-71				
M	DEAN 5-7-71				
Q1	TC08-00017	10			
N	COLE 7/28/71				
L	4-8-71 7/28/71				

CHK: O SHEPARD	DATE: 6/24/69	EQUIPMENT CORPORATION MAYFIELD, MASSACHUSETTS
OWNED BY: N SHEPARD	DATE: 7/24/69	
ENG: O LAZUKA	DATE: 2/24/69	TITLE: ERRORS
PROJ ENG: O LAZUKA	DATE: 2/2/69	
PROD: F LASKY	DATE: 3/2/69	
FIRST USED ON: TC08		
SCALE: 1 OF 1	SIZE CODE: D BS	NUMBER: TC08-3-6
SHEET: 1	DIST:	REV: E

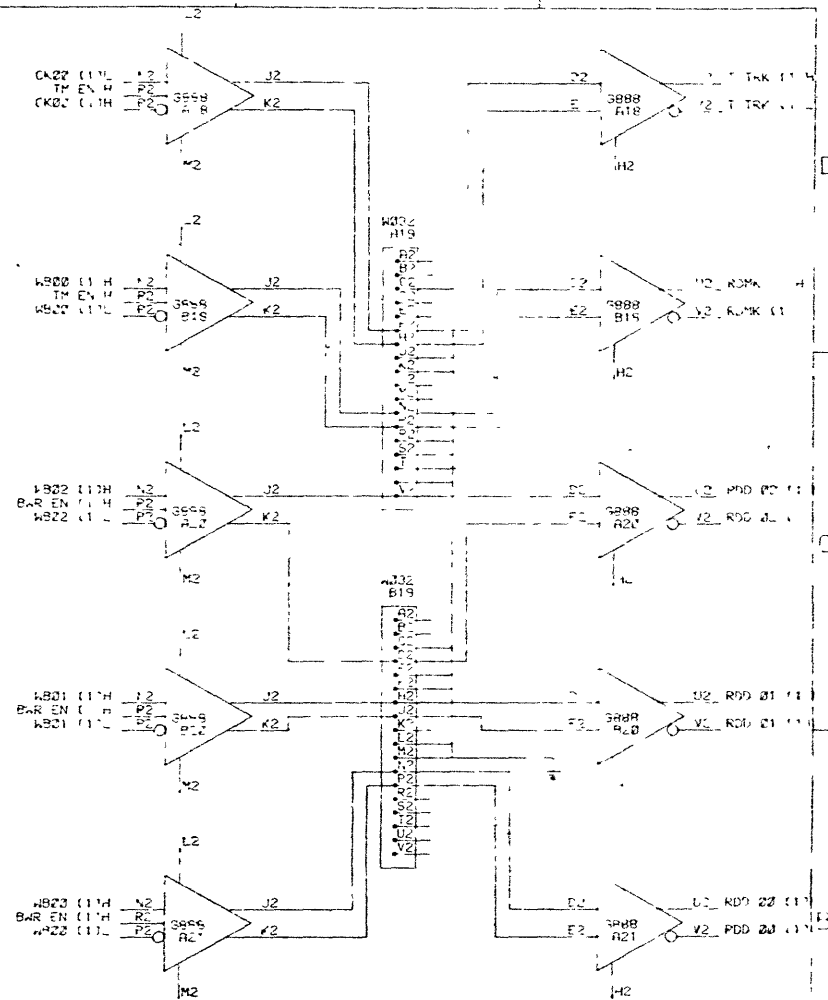
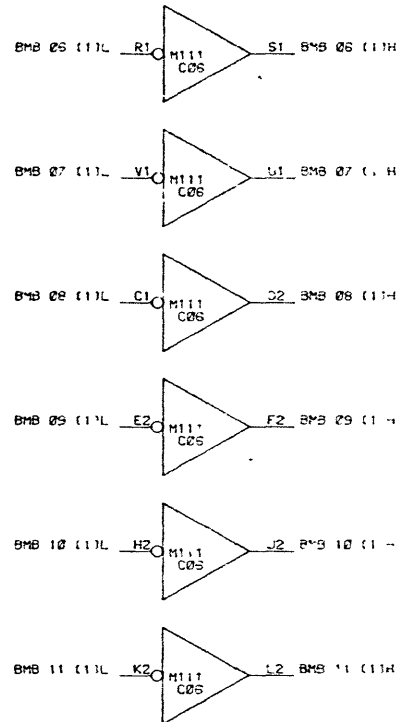
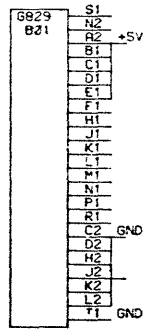
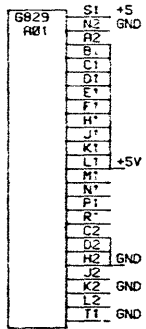
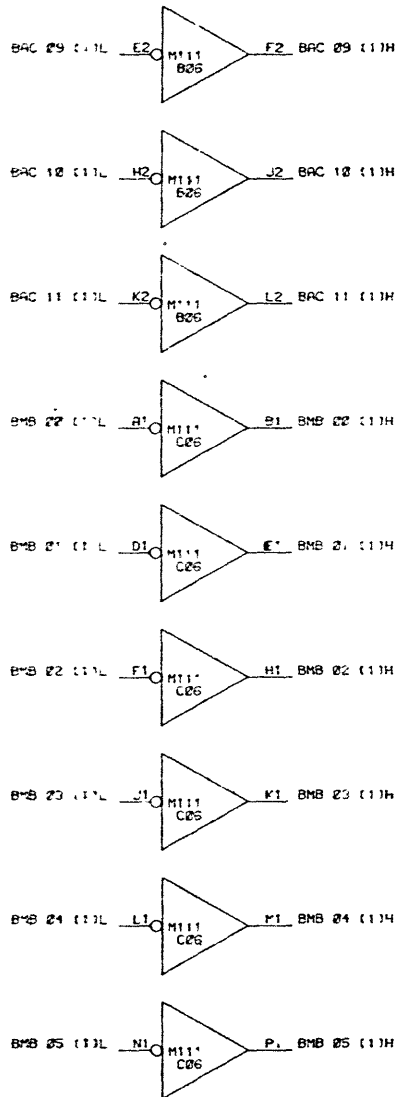
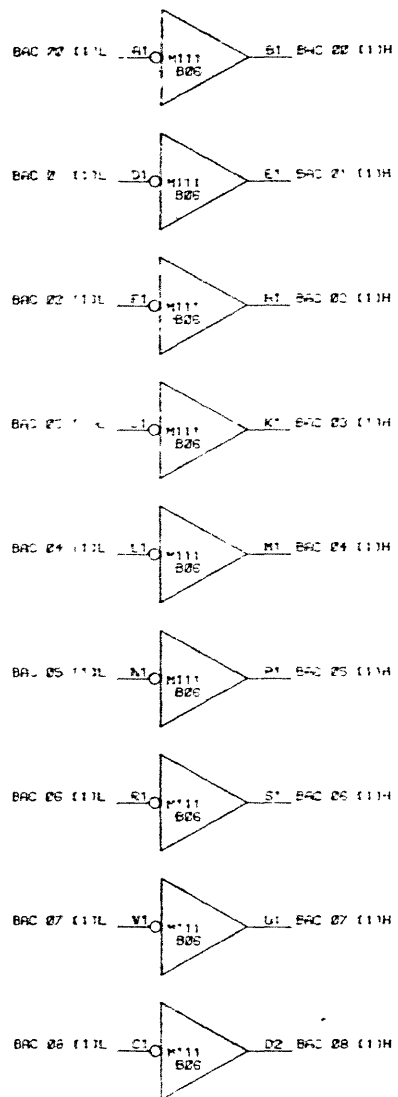
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REVISIONS		
CHK	CHANGE NO.	REV.
CH	TCCB-0001B	A
N. LEGERE		
D21 TCCB-00023		
KIRK		

DRN D SHEPARD	DATE 5-2-69	digital EQUIPMENT CORPORATION WATSON, MASSACHUSETTS
CHK N REAULT	DATE 5-3-69	
ENG D I AZUKA	DATE 9-2-69	TITLE MARK TRACK DECODE
PRD F LASKEY	DATE 9-2-69	
FIRST USED ON TCCB		
SCALE D B S	SIZE CODE TC08-0-7	NUMBER B
SHEET 1 OF 1	DIST	

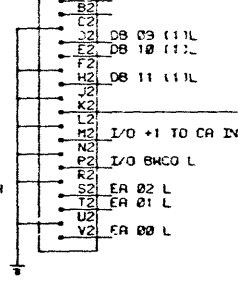
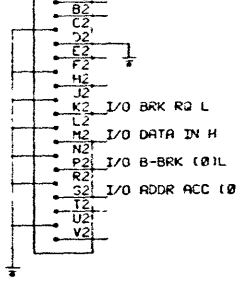
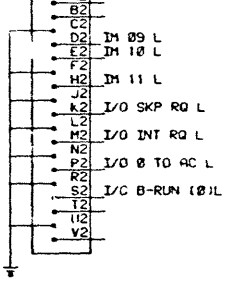
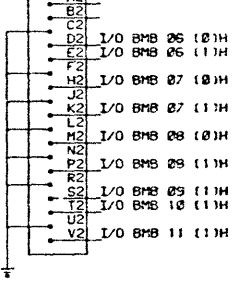
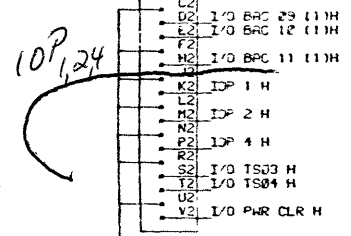
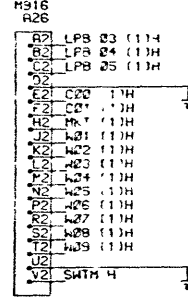
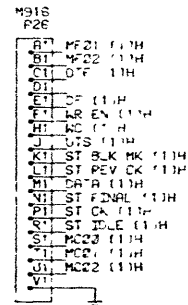
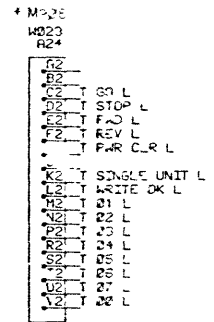
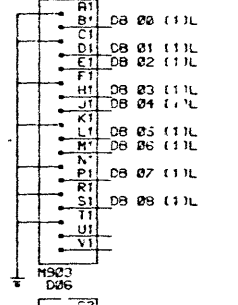
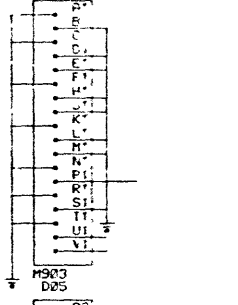
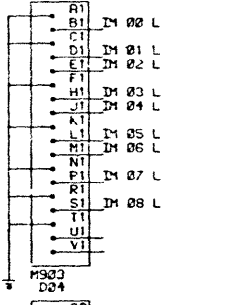
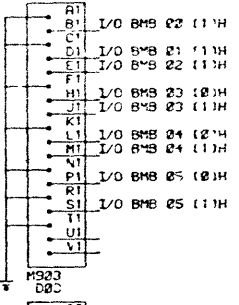
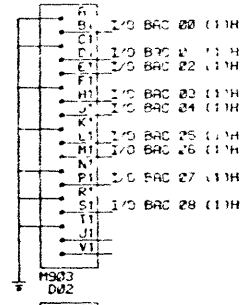
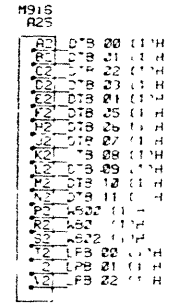
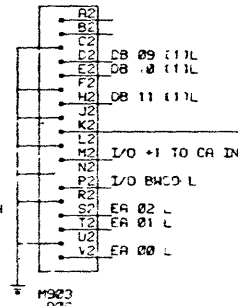
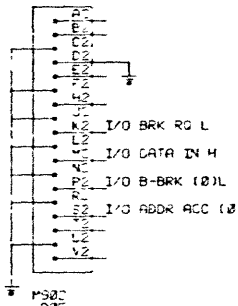
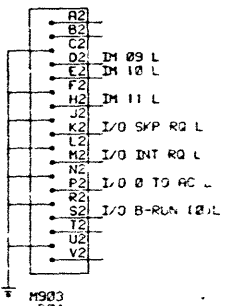
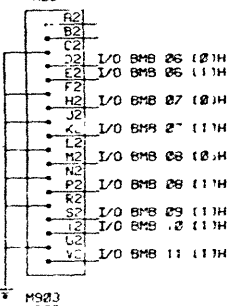
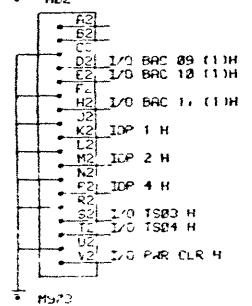
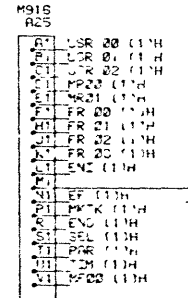
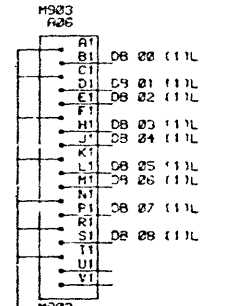
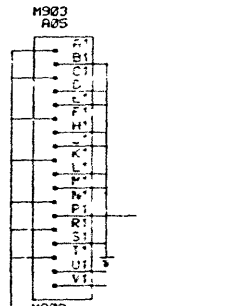
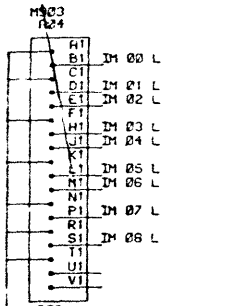
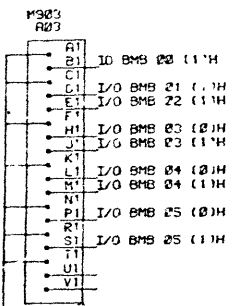
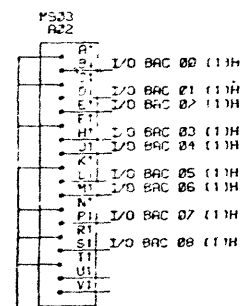
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REVISIONS		
CHK	CHANGE NO.	REV.
PC	IC29-20225	A
	A CODE 4-10-72	
	B LAZUKA 4-14-72	
	IC29-20224	B
	LAZUKA 5-7-72	

DRN D. SHEPARD	DATE 5/24/72	digital EQUIPMENT CORPORATION MADE IN MASSACHUSETTS
CHKD N. PHEAULT	DATE 5/24/72	
ENG E. LAZUKA	DATE 5-14-72	TITLE IC 29 B15 D1'S READ WRITE AMPS
PROJ. ENG C. LAZUKA	DATE 5/2/72	
PROD. E. LASKEY	DATE 5/2/72	
FIRST USED ON IC29	SCALE 1 OF 1	SIZE CODE CST
	NUMBER TC29-2-10	REV. B

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* M-03 FOR TU50 CR, FOR TU55

CHK	CHANGE NO.	REV
NR	TC08-02001	1P
	R SDFKA 1.1-2-69	
	D LAZUKA	
	TC08-02004	6
	CC 5-1-69	
	LAZUKA	
	THORNTON	

DRW	D. SHEPARD	DATE	5/24/69
CHKD	N. RHEAULT	DATE	5/24/69
ENK	D. LAZUKA	DATE	5/24/69
PROJ ENG	D. LAZUKA	DATE	5/2/69
PROD	F. LASKY	DATE	5/2/69

FIRST USED ON			
TC08	SCALE	DIST	REV.
	1/1	TC08-0-12	C
SHEET	1	OF	1

MODULE LDC	UTILIZATION TYPE	LIST SECT	TC08 DWG-SHEET-COORDS	REVI	7-JUL-71	21:12 SECT	PAGE: 1 DWG-SHEET-COORDS	UNUSED MODULE SECTIONS
A01	G821	S1	TC10-1-39,135					
A02	M903	A1	TC12-1-163,20			A2	TC12-1-120,20	
A03	M903	A1	TC12-1-163,55			A2	TC12-1-120,55	
A04	M903	A1	TC12-1-163,90			A2	TC12-1-120,90	
A05	M903	A1	TC12-1-163,125			A2	TC12-1-120,125	
A06	M903	A1	TC12-1-163,160			A2	TC12-1-120,160	
A07	M161	M1	TC02-1-164,80					
A08	M206	E1	TC06-1-147,170			M2	TC06-1-150,300	
		L1	TC06-1-90,300			P2	TC06-1-147,130	
		S1	TC06-1-83,120			V2	TC04-1-170,170	
A09	M117	E1	TC06-1-130,40			J2	TC06-1-133,100	V1
		L1	TC06-1-156,275			P2	TC06-1-30,152	
		S1	TC06-1-133,237			U1	TC02-1-188,130	
		V2	TC09-1-193,220					
A10	M113	C1	TC05-1-180,230			F1	TC05-1-160,230	V1 U1
		F2	TC06-1-47,40			K1	TC06-1-155,250	
		K2	TC06-1-42,70			N1	TC06-1-89,97	
		N2	TC02-1-54,170			S1	TC06-1-81,30	
		S2	TC06-1-113,230			V2	TC06-1-111,260	
A11	M111	B1	TC06-1-147,65			D2	TC06-1-80,55	
		E1	TC06-1-108,256			F2	TC06-1-39,110	
		M1	TC06-1-37,175			J2	TC06-1-52,234	
		K1	TC06-1-35,235			L2	TC01-1-147,260	
		M1	TC05-1-51,140			N2	TC05-1-109,105	
		P1	TC02-1-51,204			R2	TC03-1-185,145	
		S1	TC02-1-33,204			T2	TC09-1-180,250	
		U1	TC04-1-97,175			V2	TC03-1-119,145	
A12	M113	C1	TC06-1-55,200			F1	TC06-1-38,200	V1 U1
		F2	TC05-1-92,47			K1	TC01-1-40,160	
		K2	TC05-1-80,40			N1	TC01-1-38,135	
		N2	TC05-1-120,47			S1	TC01-1-30,160	

MODULE LDC	UTILIZATION TYPE	LIST SECT	TC08 DWG-SHEET-COORDS	REVI	7-JUL-71	21:12 SECT	PAGE: 2 DWG-SHEET-COORDS	UNUSED MODULE SECTIONS
A12	M113	S2	TC05-1-110,40			V2	TC05-1-112,70	
A14	M302	F2	TC03-1-188,100			T2	TC03-1-118,100	
A15	M527	E1	TC03-1-143,110			J2	TC03-1-99,110	V1 U1
		L1	TC03-1-150,145			P2	TC03-1-102,145	
		S1	TC03-1-165,225			V2	TC03-1-94,225	
A16	M602	F2	TC03-1-140,60			L2	TC03-1-162,185	
A18	G888	J2	TC10-1-190,240			U2	TC10-1-190,300	
A19	M332	A2	TC10-1-137,270					A1
A20	G888	J2	TC10-1-130,240			U2	TC10-1-130,300	
A21	G888	J2	TC10-1-70,240			U2	TC10-1-70,300	
A22	M502	E2	TC02-1-190,270					P2
A23	M633	D1	TC02-1-150,270			M2	TC02-1-100,270	
		K1	TC02-1-140,270			N2	TC02-1-80,270	
		R1	TC02-1-120,270			J2	TC02-1-60,270	
A24	M323	A2	TC12-1-70,200					
A25	M916	A1	TC12-1-164,250			A2	TC12-1-120,250	
A26	M916	A1	TC12-1-76,250			A2	TC12-1-32,250	
B01	G821	S1	TC10-1-30,170					
B02	M623	D1	TC11-1-176,30			M2	TC11-1-116,30	V1 U1
		K1	TC11-1-156,30			N2	TC11-1-96,30	
		R1	TC11-1-136,30			U2	TC11-1-76,30	
B03	M623	D1	TC11-1-176,90			M2	TC11-1-116,90	V1 U1 U2
		K1	TC11-1-156,90			N2	TC11-1-96,90	
		R1	TC11-1-136,90					

MODULE UTILIZATION LIST			TC08	REVI	7-JUL-71	21112	PAGE 3			
LOC	TYPE	SECT	DWG-SHEET-COORDS			SECT	DWG-SHEET-COORDS	UNUSED	MODULE	SECTIONS
B04	M623	D1	TC11-1-176,150			H2	TC11-1-116,150	V1	U1	U2
		K1	TC11-1-156,150			N2	TC11-1-96,150			
		R1	TC11-1-136,150							
B05	M623	D1	TC11-1-62,90			H2	TC11-1-42,150	V1	U1	U2
		K1	TC11-1-42,90			N2	TC11-1-42,30			
		R1	TC11-1-62,150							
B06	M111	B1	TC10-1-176,30			D2	TC10-1-32,30	V2		
		E1	TC10-1-158,30			F2	TC10-1-176,100			
		H1	TC10-1-140,30			J2	TC10-1-158,100			
		K1	TC10-1-122,30			L2	TC10-1-140,100			
		M1	TC10-1-104,30			N2	TC01-1-110,50			
		P1	TC10-1-86,30			R2	TC05-1-40,30C			
		S1	TC10-1-68,30			T2	TC01-1-30,260			
		U1	TC10-1-50,30							
B07	M207	E1	TC02-1-140,20			H2	TC02-1-140,60			
		L1	TC02-1-140,100			P2	TC02-1-140,140			
		S1	TC02-1-88,20			V2	TC02-1-88,60			
B08	M113	C1	TC08-1-190,107			F1	TC08-1-132,107	U1		
		F2	TC08-1-76,47			K1	TC08-1-76,107			
		K2	TC02-1-118,210			N1	TC08-1-190,47			
		N2	TC02-1-108,210			S1	TC08-1-132,47			
		S2	TC01-1-33,230			V1	TC05-1-45,278			
		V2	TC04-1-130,150							
B09	M206	E1	TC08-1-170,120			H2	TC08-1-112,120			
		L1	TC08-1-54,120			P2	TC08-1-170,60			
		S1	TC08-1-112,60			V2	TC08-1-56,60			
B10	M627	E1	TC05-1-83,70			J2	TC04-1-90,260	V1	U1	P2
		L1	TC05-1-54,100			S1	TC04-1-160,150			
		V2	TC01-1-120,260							
B11	M115	D1	TC05-1-66,170			H2	TC05-1-76,193			
		J1	TC05-1-57,70			M2	TC05-1-160,295			
		N1	TC05-1-55,40			S2	TC02-1-36,170			
		U1	TC05-1-65,47			V1	TC05-1-100,140			
B12	M117	E1	TC05-1-86,170			J2	TC04-1-54,35	V1		
		L1	TC05-1-76,170			P2	TC04-1-73,62			
		S1	TC04-1-140,59			U1	TC04-1-192,309			
		V2	TC04-1-119,61							
B13	M206	E1	TC04-1-170,220			H2	TC04-1-170,245			

MODULE UTILIZATION LIST			TC08	REVI	7-JUL-71	21112	PAGE 4			
LOC	TYPE	SECT	DWG-SHEET-COORDS			SECT	DWG-SHEET-COORDS	UNUSED	MODULE	SECTIONS
B13	M206	L1	TC04-1-170,270			P2	TC04-1-130,180			
		S1	TC04-1-130,220			V2	TC04-1-130,260			
B14	M206	E1	TC02-1-140,210			P2	TC02-1-177,210	L1	H2	
		S1	TC03-1-130,300			V2	TC03-1-176,300			
B15	M113	F1	TC03-1-140,30			F2	TC03-1-116,31	V1	U1	V2
		K1	TC04-1-146,160			N1	TC05-1-40,40	N2	K2	C1
		S1	TC05-1-170,140			S2	TC05-1-158,260			
B16	M602	F2	TC03-1-192,60			L2	TC03-1-100,185			
B18	G888	J2	TC10-1-100,240			U2	TC10-1-160,300			
B19	M332	A2	TC10-1-85,270					A1		
B20	G888	J2	TC10-1-100,240			U2	TC10-1-100,300			
B21	G879	P1	TC05-1-0,0			P1	TC06-1-0,0			
B22	M633	U2	TC02-1-40,270					N2	H2	R1
								K1	D1	
B23	M305	D2	TC02-1-172,286			E2	TC02-1-162,286	F2		
		H2	TC02-1-152,286			J2	TC02-1-142,286			
		K2	TC02-1-132,286			L2	TC02-1-122,286			
		M2	TC02-1-122,286			N2	TC02-1-112,286			
		P2	TC02-1-102,286			R2	TC02-1-92,286			
		S2	TC02-1-82,286			T2	TC02-1-72,286			
		U2	TC02-1-62,286			V2	TC02-1-42,286			
C02	M101	B1	TC11-1-156,210			E1	TC11-1-176,210			
		F2	TC11-1-136,210			H1	TC11-1-166,210			
		J2	TC11-1-96,210			K1	TC11-1-156,210			
		L2	TC11-1-86,210			M1	TC11-1-146,210			
		N2	TC11-1-76,210			P1	TC11-1-136,210			
		R2	TC11-1-66,210			S1	TC11-1-176,210			
		T2	TC11-1-56,210			U1	TC11-1-116,210			
V2	TC11-1-46,210									
C03	M101	B1	TC11-1-186,270			E1	TC11-1-176,270	V2	T2	R2
		F2	TC11-1-166,270			H1	TC11-1-166,270			

MODULE UTILIZATION LIST			TC08	REVI	7-JUL-71	21:12	PAGE 5	UNUSED MODULE SECTIONS		
LOC	TYPE	SECT	DWG-SHEET=COORDS			SECT	DWG-SHEET=COORDS			
C03	M101	J2	TC11-1-98,270			K1	TC11-1-158,270			
		L2	TC11-1-89,270			M1	TC11-1-146,270			
		N2	TC11-1-78,270			P1	TC11-1-136,270			
		S1	TC11-1-126,270			U1	TC11-1-116,270			
C04	M103	B1	TC01-1-170,70			K1	TC01-1-129,30	V1	N1	
C05	M103	B1	TC01-1-70,80			K1	TC01-1-30,30	V1	N1	
C06	M111	B1	TC10-1-122,100			D2	TC10-1-140,180			
		E1	TC10-1-104,130			F2	TC10-1-122,180			
		M1	TC10-1-88,100			J2	TC10-1-104,180			
		K1	TC10-1-68,100			L2	TC10-1-88,180			
		M1	TC10-1-50,100			N2	TC01-1-127,110			
		P1	TC10-1-32,100			R2	TC01-1-30,90			
		S1	TC10-1-176,190			T2	TC01-1-110,120			
		U1	TC10-1-158,180			V2	TC01-1-90,120			
C07	M207	E1	TC02-1-88,100			M2	TC02-1-88,140	V2	S1	
		L1	TC02-1-88,180			P2	TC02-1-140,180			
C08	M121	E1	TC08-1-190,227			J2	TC08-1-190,167	V1		
		L1	TC08-1-132,227			P2	TC08-1-132,167			
		S1	TC08-1-78,227			U1	TC01-1-180,260			
		V2	TC08-1-78,167							
C09	M206	E1	TC08-1-170,240			M2	TC08-1-112,240			
		L1	TC08-1-54,240			P2	TC08-1-170,180			
		S1	TC08-1-112,180			V2	TC08-1-58,180			
C10	M121	E1	TC08-1-176,277			J2	TC09-1-30,103	V1	U1	
		L1	TC08-1-118,277			P2	TC06-1-175,252			
		S1	TC08-1-62,277			V2	TC09-1-32,230			
C11	M113	C1	TC04-1-150,35			F1	TC04-1-130,35	V1	U1	
		F2	TC04-1-136,82			K1	TC04-1-120,35			
		K2	TC09-1-110,50			N1	TC04-1-114,58			
		N2	TC04-1-130,250			S1	TC04-1-130,82			
		S2	TC04-1-74,127			V2	TC04-1-70,150			
C12	M115	D1	TC03-1-35,223			M2	TC09-1-90,50			
		J1	TC04-1-119,105			M2	TC03-1-30,40			

MODULE UTILIZATION LIST			TC08	REVI	7-JUL-71	21:12	PAGE 6	UNUSED MODULE SECTIONS			
LOC	TYPE	SECT	DWG-SHEET=COORDS			SECT	DWG-SHEET=COORDS				
C12	M115	N1	TC04-1-84,35			S2	TC03-1-80,37				
		U1	TC04-1-74,35			V1	TC04-1-64,35				
C13	M111	B1	TC04-1-44,80			D2	TC05-1-73,216				
		E1	TC05-1-140,140			F2	TC05-1-140,260				
		M1	TC05-1-120,140			J2	TC05-1-117,299				
		K1	TC05-1-140,200			L2	TC05-1-97,290				
		M1	TC05-1-120,200			N2	TC03-1-51,246				
		P1	TC03-1-69,95			R2	TC09-1-37,80				
		S1	TC04-1-54,200			T2	TC09-1-187,80				
		U1	TC04-1-67,175			V2	TC02-1-165,185				
C14	M206	E1	TC08-1-170,300			M2	TC08-1-112,300	V2			
		L1	TC08-1-58,300			P2	TC03-1-65,260				
		S1	TC05-1-36,240								
C15	M113	C1	TC05-1-150,47			F1	TC05-1-140,40	V1			
		F2	TC09-1-40,37			K1	TC05-1-142,70				
		K2	TC09-1-190,50			N1	TC03-1-70,30				
		N2	TC09-1-190,140			S1	TC03-1-72,80				
		S2	TC03-1-65,233			U1	TC03-1-194,260				
		V2	TC02-1-158,192								
C16	M627	E1	TC03-1-59,290			J2	TC05-1-120,260	V1	U1		
		L1	TC03-1-50,290			P2	TC01-1-100,290				
		S1	TC03-1-170,30			V2	TC03-1-150,31				
C17	M111	B1	TC01-1-130,260			D2	TC03-1-137,82	V2	L2	U1	
		F2	TC03-1-99,82			M1	TC05-1-37,76	E1			
		J2	TC06-1-124,295			K1	TC05-1-97,165				
		M1	TC05-1-167,159			N2	TC09-1-27,130				
		P1	TC01-1-60,260			R2	TC09-1-177,170				
		S1	TC01-1-55,157			T2	TC06-1-70,300				
C18	M228		TC07-1-0,0								
D02	M903	A1	TC12-1-75,20			A2	TC12-1-32,20				
D03	M903	A1	TC12-1-75,55			A2	TC12-1-32,55				
D04	M903	A1	TC12-1-75,90			A2	TC12-1-32,90				
D05	M903	A1	TC12-1-75,125			A2	TC12-1-32,125				

MODULE	LDC	TYPE	SECT	TC08 DWG-SHEET-COORDS	REVI	SECT	TC08 DWG-SHEET-COORDS	UNUSED MODULE SECTIONS
D05	M903							
D06	M903	A1		TC12-1-75,160		A2	TC12-1-32,160	
D07	M161	R1		TC02-1-34,70				
D08	M207	E1		TC09-1-136,180		H2	TC09-1-136,290	
		L1		TC09-1-96,180		P2	TC09-1-96,290	
		S1		TC09-1-56,180		V2	TC09-1-56,290	
D09	M121	E1		TC09-1-145,150		J2	TC09-1-145,260	V1
		L1		TC09-1-105,150		P2	TC09-1-103,260	
		S1		TC09-1-65,150		U1	TC02-1-170,130	
		V2		TC09-1-65,260				
D10	M119	J2		TC04-1-57,150		P2	TC03-1-50,100	U1
		V1		TC04-1-192,255		V2	TC09-1-160,50	
D11	M206	E1		TC01-1-180,140		H2	TC01-1-180,170	
		L1		TC01-1-180,230		P2	TC04-1-170,50	
		S1		TC01-1-180,230		V2	TC04-1-170,100	
D12	M627	E1		TC01-1-147,160		J2	TC09-1-60,50	V1 U1
		L1		TC01-1-77,160		P2	TC09-1-104,73	
		S1		TC01-1-80,120		V2	TC01-1-100,144	
D13	M602	F2		TC01-1-150,130		L2	TC01-1-150,210	
D14	M307	H2		TC03-1-80,160		K1	TC03-1-49,150	
D15	M401	E2		TC03-1-178,260				
D16	M302	T2		TC06-1-73,255				F2
D17	M602	F2		TC01-1-58,135		L2	TC04-1-38,40	
D18	M228			TC07-1-0,0				
D19	M112	A1		TC04-				K1, M1, S1, U1, W1 FL, RL, NL, GL, V2
		F1		TC04-				

TYPE	USED	SECT USED	TC08 SECT LEFT	DESC
G821	1	1	1	
G879	0	SPEC	MDD	
G888	9	10	0	READER/WRITER
M101	2	23	7	JIDGE GATE
M103	2	4	4	
M111	5	65	15	
M113	6	58	14	JIDGE GATE
M115	2	16	0	8-3 INPUT NAND GATES
M117	2	14	2	8-4 NAND GATES
M119	1	4	1	8-INPUT NAND GATES
M121	3	20	4	X OR GATES
M161	2	2	0	BINARY TO OCTAL/DECIMAL DECODER
M206	7	39	3	SIX FLIP-FLOPS
M207	3	16	2	FLIP-FLOP
M228	1	SPEC	MDD	
M302	2	3	1	ONE SHOT DELAY
M307	1	2	0	
M401	1	1	0	CLOCK
M502	1	1	1	NEGATIVE INPUT CONVERTER
M602	4	8	0	PULSE GENERATOR
M623	4	21	11	JIDGE GATE
M677	4	23	9	8-4 NAND GATES
M633	2	7	5	JIDGE GATE
M903	10	20	0	
M916	2	4	0	CONNECTOR BOARD
W005	1	14	1	CLAMP LOAD
W023	1	1	0	CONNECTOR BOARD
W032	2	2	2	CONNECTOR BOARD
M112	1	1	8	NOR GATE


DRWG NO

REVLTR

K-WL-TCØ8-Ø-14

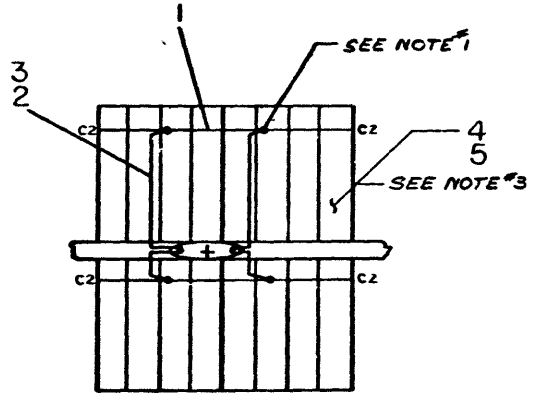
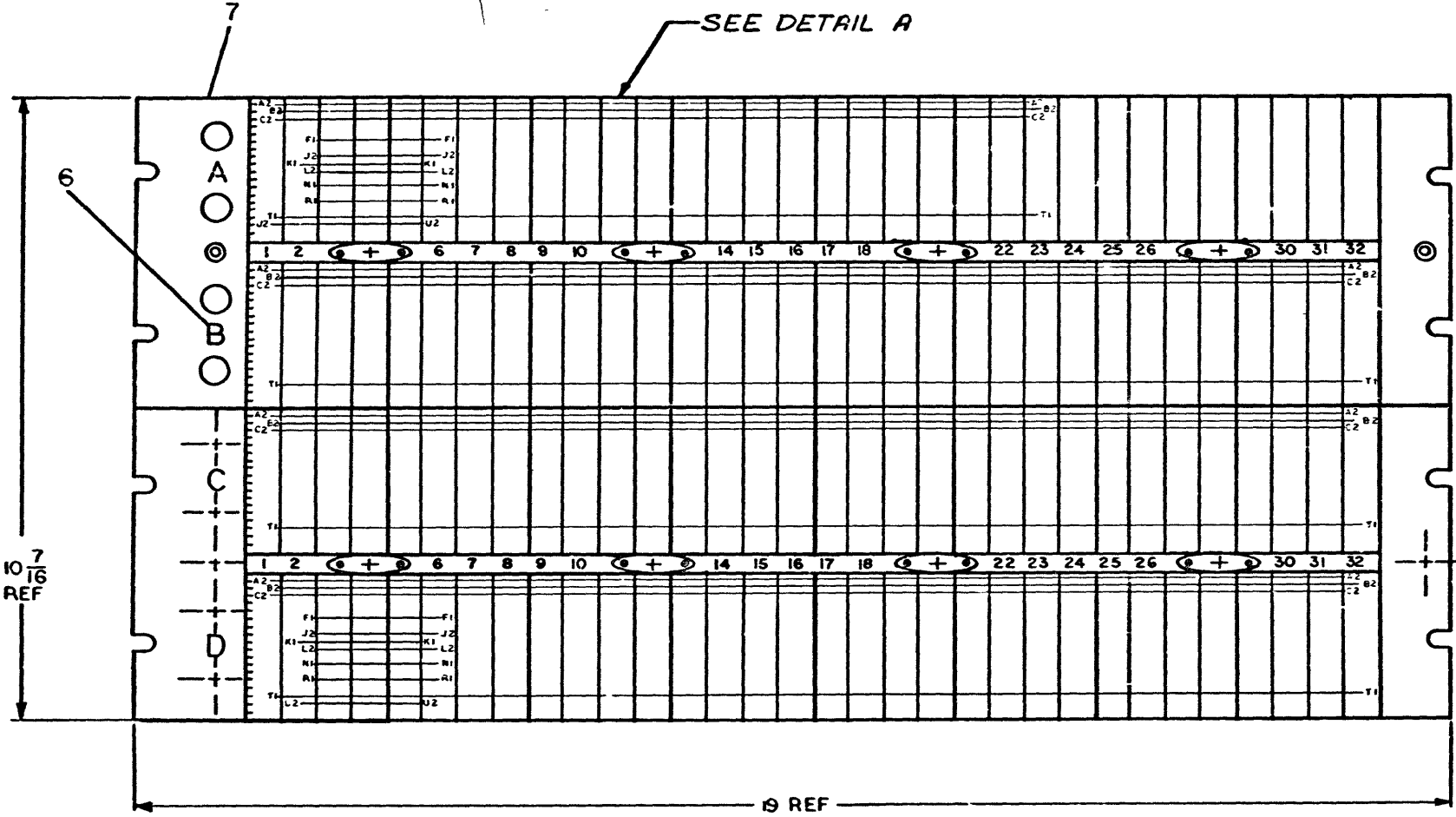
T

REVISIONS			
REV LTR	ECD NO	DATE	ENG
A	TCØ8-00001	11-17-70	W
B	TCØ8-00002	11-17-70	W
C	TCØ8-00004	11-17-70	W
D	TCØ8-00005	3-27-71	RZ
E	TCØ8-00006	4-24-70	W
F	00008	7-7-70	W
H	TCØ8-00009	1-30-71	W
J	TCØ8-00010	10-11-70	W
K	TCØ8-00012	11-12-70	W
L	TCØ8-00014	2-11-71	W
M	TCØ8-00015	6-10-71	W
N	TCØ8-00016	6-11-71	W
P	TCØ8-00018	8-25-71	W
R	TCØ8-00021	1-1-71	W
S	TCØ8-00023	1-23-71	W
T	TCØ8-00026	10-24-71	W

DRAWN <i>G. Krasinski</i>		DATE 6/12/69		 digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS	TITLE WIRE LIST TCØ8	
CHECKED <i>H. J. ...</i>		DATE 6/15/69			FOR TAPE* FILE*	
ENG <i>H. J. ...</i>		DATE 1-25-71			SIZE CODE DWG. NO.	
PROJ ENG <i>H. J. ...</i>		DATE 1-25-71			K WL TCØ8-Ø-14	
PROD <i>H. J. ...</i>		DATE 9/15/69		ASSY NO		REV LTR
SCALE NONE				SHEET 1 OF 1		DIST

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- NOTES:**
1. CONNECTIONS ON ITEMS #1 & #2 TO BE SOLDERED AND LOCATED AT MINIMUM PRACTICAL HEIGHT ABOVE BOARD.
 2. ALL CONN BLOCKS TO BE GROUNDED TO GND LUGS AS SHOWN.
 3. USE YELLOW WIRE (ITEM #4) FOR MACHINE WRAPPED & BLUE WIRE (ITEM #5) FOR HAND WRAPPED WIRING.



REV.	DATE	BY	CHKD.
A	6-13-68	J. G. ...	J. G. ...
B	6-13-68	J. G. ...	J. G. ...
C	6-13-68	J. G. ...	J. G. ...
D	6-13-68	J. G. ...	J. G. ...
E	6-13-68	J. G. ...	J. G. ...
F	6-13-68	J. G. ...	J. G. ...
G	6-13-68	J. G. ...	J. G. ...
H	6-13-68	J. G. ...	J. G. ...
I	6-13-68	J. G. ...	J. G. ...
J	6-13-68	J. G. ...	J. G. ...
K	6-13-68	J. G. ...	J. G. ...
L	6-13-68	J. G. ...	J. G. ...
M	6-13-68	J. G. ...	J. G. ...
N	6-13-68	J. G. ...	J. G. ...
O	6-13-68	J. G. ...	J. G. ...
P	6-13-68	J. G. ...	J. G. ...
Q	6-13-68	J. G. ...	J. G. ...
R	6-13-68	J. G. ...	J. G. ...
S	6-13-68	J. G. ...	J. G. ...
T	6-13-68	J. G. ...	J. G. ...
U	6-13-68	J. G. ...	J. G. ...
V	6-13-68	J. G. ...	J. G. ...
W	6-13-68	J. G. ...	J. G. ...
X	6-13-68	J. G. ...	J. G. ...
Y	6-13-68	J. G. ...	J. G. ...
Z	6-13-68	J. G. ...	J. G. ...

QTY	DESCRIPTION	PART NO	ITEM NO.
	TC08		
UNLESS OTHERWISE SPECIFIED			
DIMENSIONS IN INCHES			
TOLERANCES			
FRACTIONS ANGLES			
DECIMALS ± 0.005 ± 0.010			
FINISH SURFACE QUALITY			
REMOVE BURRS AND BREAK SHARP CORNERS			
UNLESS OTHERWISE SPECIFIED			
FINISH HIGHER ASSC.			
D-VA-TC08-0-0		SCALE	NONE
SHEET 1 OF 1		DIST	
DATE 6-13-68		DATE 6-13-68	DATE 6-13-68
CHKD. J. G. ...		DATE 6-13-68	DATE 6-13-68
ENGR. J. G. ...		DATE 6-13-68	DATE 6-13-68
PROD. J. G. ...		DATE 6-13-68	DATE 6-13-68
DRAWN J. G. ...		DATE 6-13-68	DATE 6-13-68
TITLE		SIZE CODE	NUMBER
WIRED ASSY		DAD7006394-0-0	C
TC08			

DAD7006394-0-0 C

**DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS**

DATE 9-29-69

TITLE TC08 & TC08N CHECKOUT PROCEDURES

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
A		TC08-00005	LAZUKA	3-21-70	L. V.	4-14-70
B		TC08-00013	NARHI	12-14-70	L. V.	1-22-71

A. EQUIPMENT REQUIREMENTS

1. TC08 Back Panel
2. TC08 Indicator System
3. TC08 or TC08N Module Kit
4. TC08 and TC08N Logic Prints
5. Set of TC01 Maindec's
6. 783 Power Supply or Equivalent
7. 716 Indicator Supply
8. Minimum of 1 TU55 or TU56 Transport
9. Dual Trace Scope

B. PRELIMINARY CHECKS

1. With all other modules removed, plug in the G821 power regulator and connect the power OK indicator across pins B01M2 and B01M2.
2. Inspect panel for discrepancies such as power bus shorts, broken module blocks, broken wires, bent or pushed in pins, and correct installation of the WRTM - normal switch.
3. By using a Mate-N-Lok connector, connect power to the regulator and apply power to the empty panel and check power bus for correct voltage.
4. Connect the 716 power supply to the indicator system and install cables. Power up the empty logic panel and the indicator system. All indicators except those that are deliberately tied to ground should be ON.

C. PRELIMINARY CHECKS AND SETUP

1. Plug in all modules and cables.
2. Test power clear for correct operation.

ENG	D. Lazuka	APPD	SIZE	CODE	NUMBER	REV
			A	SP	TC08-0-16	B

DEC FORM NO DRA 107A SHEET 1 OF 4

CONTINUATION SHEET

TITLE TC08 & TC08N CHECKOUT PROCEDURE

7. By removing the G888 in slot A18 and adding a temporary jumper between D14K2 and D14U1, and also changing address 13 of the previous program to ALL ZERO's!! The program may be used to fire the SP DY which should now be set to the value noted on the prints. After the SP DY is set, remove the jumper, insert the G888 back into slot A18, and replace the original contents of address 13 (0400). NOTE, THE LOWER SWITCH ON REV B M307 SHOULD BE SET TO POSITION 4
8. By adding the following instructions to the previous program, a tape rocking program can be produced. Start program at location 16.

```

0016 7600 CLA
0017 1023 TAD
0020 6766 DTLA
0021 5000 JMP START
0022 7402 HLT I/O SKIP
0023 0200
    
```

9. By using the following program the write timing and mark track clock may be enabled:

```

Start 0000 1004 TAD
0001 6766 DTLA
0002 6764 DTXA
0003 5002 JMP .-1
0004 0200
    
```

Place unit 8 on-line and write enabled. Place WRTM normal switch in the WRTM position. Start the program. The clock should be set to the value noted on the prints.

D. BASIC TESTING

1. The TC01 basic exerciser (Maindec-08-D3BB-D) provides a comprehensive test procedure. The tests also follow in a logical sequence of testing. If this sequence is followed, checkout time and problems will be held to a minimum.
2. After all tests of the basic exerciser have been run correctly, the DECTape formatter (DEC-08-EUFA-D) should be run.
3. DECTrex 1 (Maindec-08-D3RA-D) should be made to run error free.
4. The DECTape Library System (DEC-08-SUAL-1A) should now be tried. And made to run correctly.

	Dave Lazuka	SIZE	CODE	NUMBER	REV
		A	SP	TC08-0-16	B

DEC FORM NO DRA 108A SHEET 1 OF 1

CONTINUATION SHEET

TITLE TC08 & TC08N CHECKOUT PROCEDURE

3. Key in the following instructions

LOCATION	CODE	MNEUMONIC
0000	7604	LAS
0001	0010	AND (0017)
0002	1011	TAD (6760)
0003	3005	DCA
0004	1012	TAD (0400)
0005	7402	HLT
0006	5000	JMP START
0007	7402	HLT I/O SKIP
0008	0017	
0011	6760	
0012	0400	

This program will execute IOT instructions to device 76 or 77 IOPS 1, 2, or 4 under control of AC switch bits 8-11.

4. The IOT decoding should not be tested. By watching the outputs of the IOT decoder with a scope and placing the IOP in the switch register.
5. Place 0004 in the switch and set the XSA DY to the value noted on the prints.
6. Key in the following program:

```

Start 0000 7604 LAS
0001 7040 CMA
0002 3015 DCA
0003 2014 ISZ
0004 5003 JMP .-1
0005 2015 ISZ
0006 5003 JMP .-3
0007 1013 TAD
0008 6764 DTXA
0011 5000 JMP (START)
0012 7402 HLT I/O SKIP
0013 0400
0014 0000
0015 0000
    
```

This program causes the direction bit to XORED at a rate determined by the contents of the switch register. This program generates U M and also fires the U M DY which should now be set to the value noted on the prints. NOTE THE UPPER SWITCH ON REV B M307 SHOULD BE SET TO POSITION 1

D. Lazuka	SIZE	CODE	NUMBER	REV
	A	SP	TC08-0-16	B

DEC FORM NO DRA 108A SHEET 1 OF 1

CONTINUATION SHEET

TITLE TC08 & TC08N CHECKOUT PROCEDURE

E. ELEVATED TEMPERATURE TESTING

1. The control must run DECTrex 1 for ONE hour error free at 55° centigrade.

F. LIFE TESTING

1. With all of the transports being shipped with the system, DECTrex 1 should be run for a minimum of ONE hour per transport.

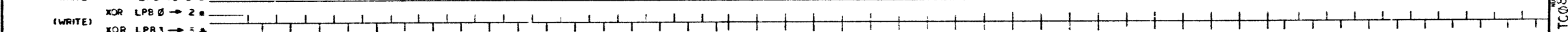
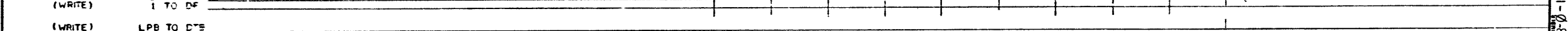
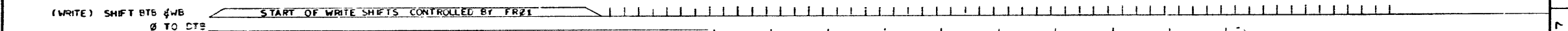
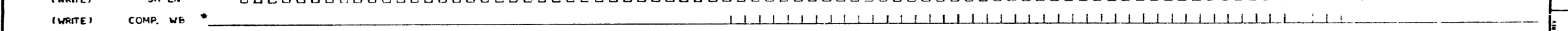
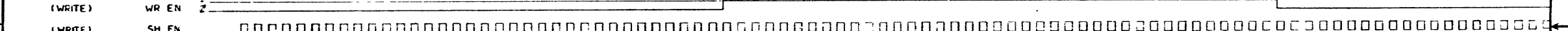
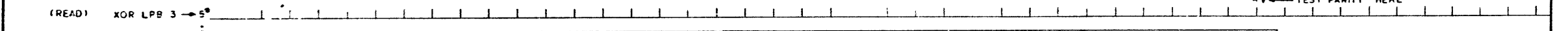
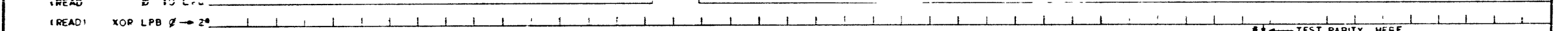
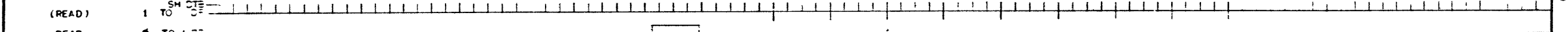
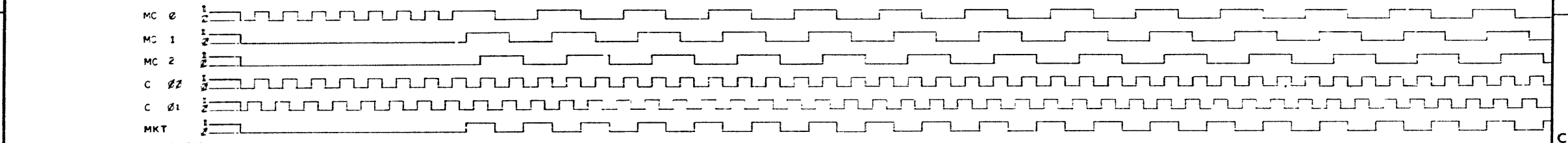
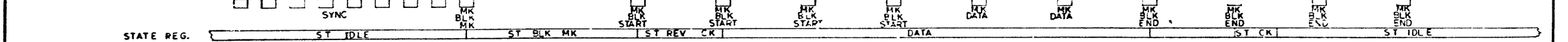
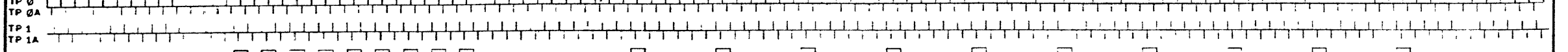
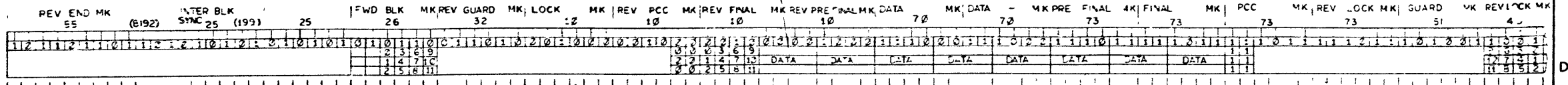
G. CLEANUP AND ADDITIONAL TESTS

1. Checkout of the control is now complete.
2. Most DECTape systems are shipped in a cabinet and the system must be run after its installation in the cabinet before acceptance.

Dave Lazuka	SIZE	CODE	NUMBER	REV
	A	SP	TC08-0-16	B

DEC FORM NO DRA 108A SHEET 1 OF 1

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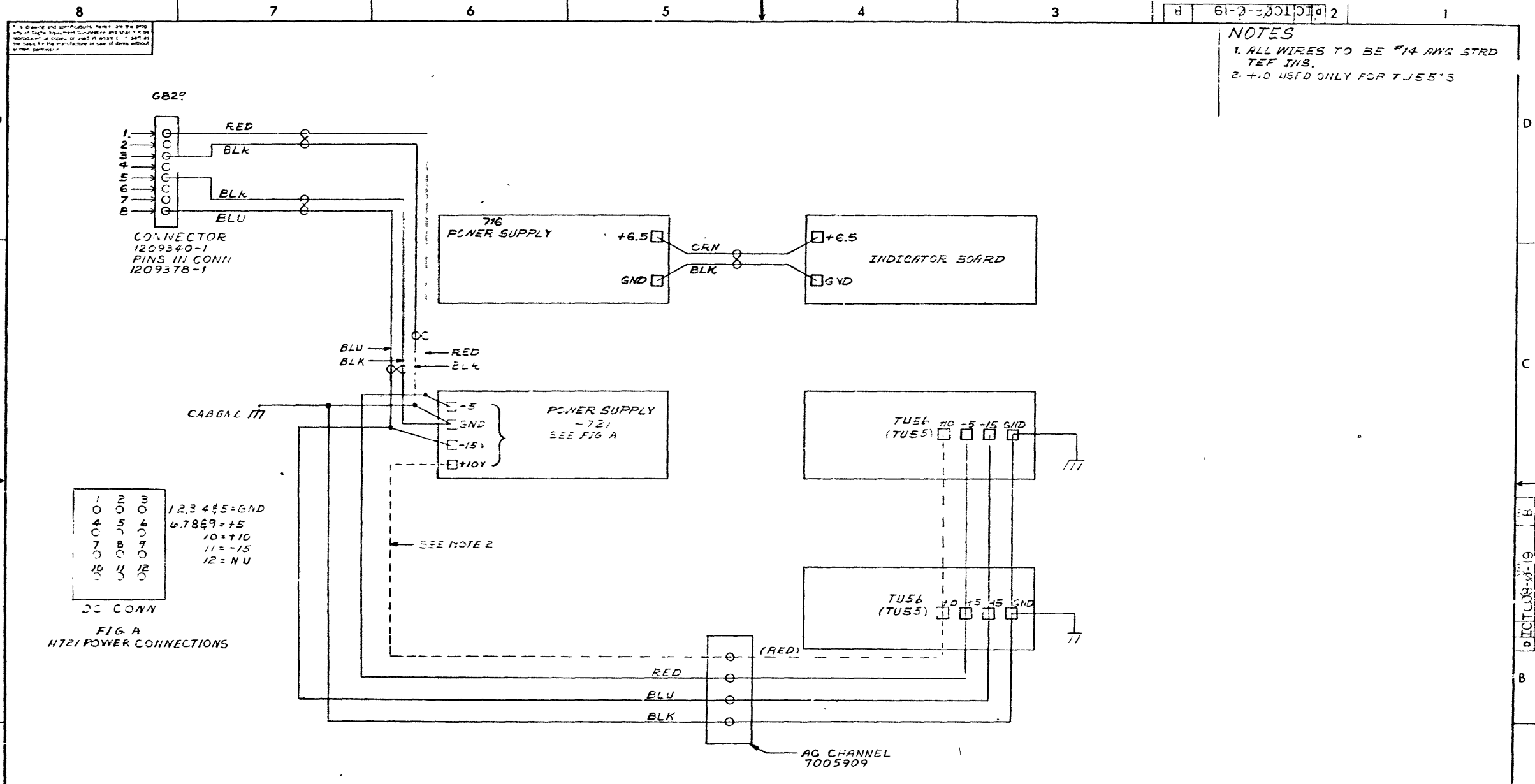


NOTE: * SIGNAL DOES NOT EXIST AS SUCH BUT IS A GRAPHIC REPRESENTATION OF IT TIME AND FUNCTION.

REV
CHANGE NO
REVISIONS
CHE

QTY	DESCRIPTION	PART NO	ITEM NO
PARTS LIST			
UNLESS OTHERWISE SPECIFIED		DRN	DATE
UNLESS OTHERWISE SPECIFIED		CHK D	DATE
TOLERANCES		ENG	DATE
DECIMALS FRACTIONS ANGLES		PROJ ENG	DATE
= .005 ± 1/64 ± 0°30'		PROD	DATE
FINAL SURFACE QUALITY			
REMOVE BURRS AND BREAK SHARP CORNERS			
MATERIAL	FIRST USED ON		
FINISH	SCALE	SHEET	OF
TITLE		SIZE CODE	NUMBER
TC08 TIMING		DITD	TC08-0-17
		DIST	REV

REV
TC08-0-17
DITD



NOTES
 1. ALL WIRES TO BE #14 AWG STRD TEF INS.
 2. +10 USED ONLY FOR TUS5'S

1	2	3	
0	0	0	1,2,3,4,5 = GND
4	5	6	6,7,8,9 = +5
7	8	9	10 = +10
10	11	12	11 = -15
0	0	0	12 = NU

DC CONN
 FIG A
 H721 POWER CONNECTIONS

REV	NO	DATE	BY
1	1	1/1/71	LLJ/USA
2	1	1/1/71	LLJ/USA
3	1	1/1/71	LLJ/USA
4	1	1/1/71	LLJ/USA
5	1	1/1/71	LLJ/USA
6	1	1/1/71	LLJ/USA
7	1	1/1/71	LLJ/USA
8	1	1/1/71	LLJ/USA

FIRST USED ON OPTION/MODEL
 TC08

DO NOT SCALE DRAWING UNLESS OTHERWISE SPECIFIED DIMENSION IN INCHES	DRY CHKD ENG PROJ. ENGR DATE 1/1/71	CITY DATE 1/1/71	PARTS LIST
TOLERANCES DECIMALS FRACTIONS ANGLES ± .005 ± .010 ± .015 FINAL SURFACE QUALITY REMOVE BURRS AND BREAK SHARP CORNERS	MATERIAL FINISH	NEXT HIGHER ASSY D-L-T08-2-2	TITLE TC08 SYSTEM DC POWER WIRING (TUS5 OR TUS6)
SCALE 1 OF 1	SIZE/CODE DST	NUMBER 6	ITEM NO. 6

DICT08-2-19

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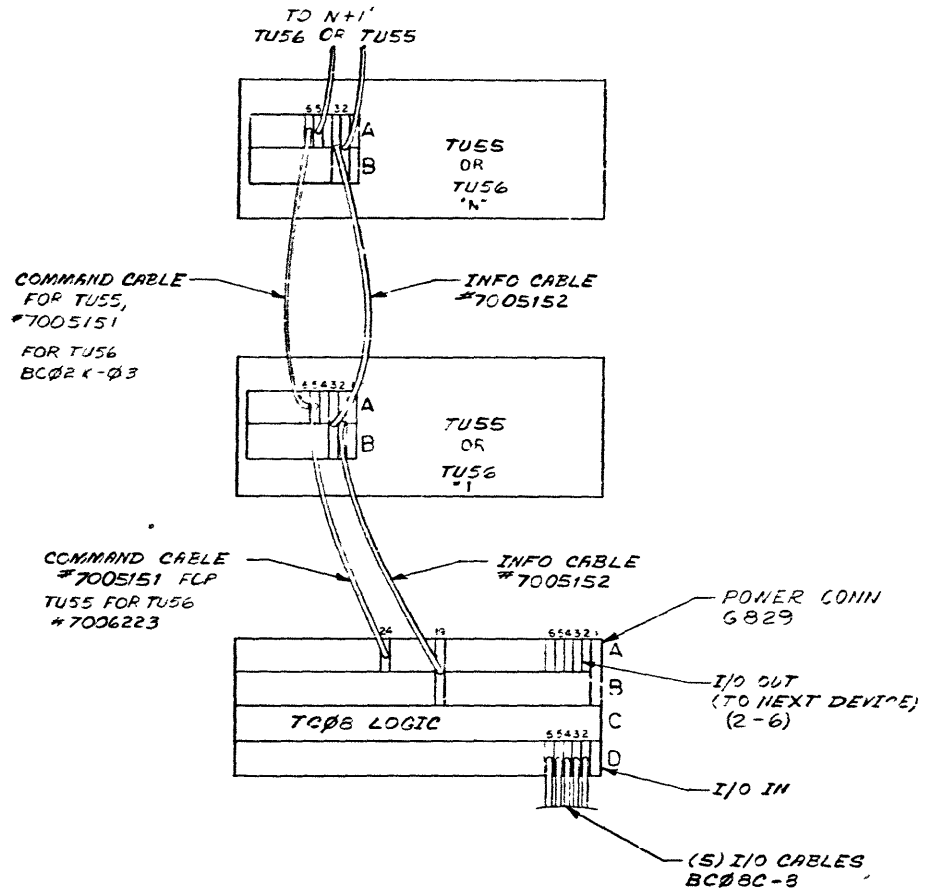
CONNECTION TABLE FOR TU55/TU56 TO TU55/TU56

CABLE TYPE	FROM		TO	
	TU55	TU56	TU55	TU56
7005152	AB02 AB03	AB10 OR AB11	AB02 OR AB03	AB10 OR AB11
7005151	A05 OR A06	A06 OR A07	A05 OR A06	A06 OR A07
BC02X03	NOT USED	A06 OR A07	NOT USED	A06 OR A07

CONNECTION TABLE FOR TU55/TU56 TO TC03

CABLE TYPE	TU55 LOCATION	TU56 LOCATION	TC03 LOCATION
7005152	AB02 OR AB03	AB10 OR AB11	AB19
7005151	A05 OR A06	A06 OR A07	A24
7006223	NOT USED	A06 OR A07	A24

NOTE:
WHEN INTERMIXING TU55'S WITH TU56'S, TU56'S MUST ALWAYS BE FIRST AFTER THE TC03 WHEN CABLEING UP THE SYSTEM, EG TC03 → TU56 → TU55
TD TC03 → TU56 → TU55



REVISIONS	CHK	CHG	NO	DATE
1				

FIRST USED ON OPTION/MODEL
TC03

DO NOT SCALE DRAWING
UNLESS OTHERWISE SPECIFIED
DIMENSION IN INCHES
TOLERANCES
DECIMALS FRACTIONS ANGLES
± .005 ± .001 ± .030
FINAL SURFACE QUALITY
REMOVE BURRS AND BREAK SHARP CORNERS
MATERIAL
FINISH

QTY	DESCRIPTION	PART NO	ITEM NO
	TC03 SYSTEM CABLE CONFIGURATION		
	A-M-L-TC03-0-0		
	SCALE		
	SHEET 1 OF		

TC03-0-20

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION

DATE 10/2/70

TITLE TC98 Acceptance Procedure

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE

ENG	Larry Narhi	APPD	<i>Turbic</i>	SIZE	A	CODE	SR	NUMBER	TC08-0-02	REV	
-----	-------------	------	---------------	------	---	------	----	--------	-----------	-----	--

0150150

CONTINUATION SHEET

TITLE TC98 Acceptance Procedure

Purpose: To define the procedure to accept a TC98, DECTape controller for shipment.

Test hardware:

- 1) A PDP-8 family computer
- 2) One or more TU55 or TU56 tape transports
- 3) TC98 indicator panel
- 4) 716 indicator supply
- 5) 783 or equivalent supply
- 6) A TC73 or TC28-11 depending on the computer output bus polarity

Test Software:

- 1) TC91 Basic Exerciser
- 2) TC91 Random Exerciser

Procedure:

- 1) Make sure all ECO's have been installed
- 2) Perform QC inspection
- 3) Make the Basic Exerciser run on each transport
- 4) Run the Random Exerciser for a minimum of one hour for each drive that is to be shipped with the system. No errors are acceptable.
- 5) Run DECTape formatter program on each drive.
- 6) If the system has extra memory, run the DECTape Extended Memory Exerciser for 1/2 hour per drive transport.
- 7) If the system has any other Data Entry devices, run the DM91 Exerciser for a minimum of 1/2 hour.
- 8) Any standard DECTape system software may be run in acceptance at the operators discretion.

Shipping Software:

- 1) All DECTape MAI/DECS
- 2) Complete set of DECTape system software including Library system tapes.
- 3) TC98 Print set of the latest revision.

SIZE	A	CODE	SR	NUMBER	TC08-0-02	REV	
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ENGINEERING SPECIFICATION					DATE 10/1/70						
TITLE TC08 Engineering Specification											
REVISIONS											
REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE					
Table of Contents											
1.1 General Description											
1.1.1 A Computer Peripheral											
1.1.2 Stores Digital Data on 3/4 Inch Magnetic Tape											
1.1.3 Stores Data in a Three Track Serial/Parallel Format											
1.1.4 Data Can Be Accessed in Blocks											
1.1.5 Data Can Be Accessed in Both Directions											
1.2 Operational Description of DECTape											
1.2.1 The Tape Surface Recording Format											
1.2.1.1 DECTape Heads and Tape Tracks											
1.2.1.2 Tape Recording Format											
1.2.2 The DECTape Architecture											
1.2.2.1 The Control Section											
1.2.2.2 The Data Transfer Section											
1.2.2.3 The Formatter Section											
1.3 TC08 Operator Controls and Indicators											
1.4 Programming Examples											
1.4.1 Automatic Search											
1.5 Equipment Description											
1.5.1 Hardware											
1.5.2 Environmental Requirements											
1.5.3 Power Requirements											
ENG	L. Narhi	APPD	<i>[Signature]</i>	SIZE	A	CODE	TC08-1	NUMBER		REV	

ENGINEERING SPECIFICATION				CONTINUATION SHEET			
TITLE TC08 Specification							
1.1 General Description							
The DECTape system is a computer peripheral which stores digital data on 3/4 inch magnetic tape in a three track parallel/serial format, with which the data can be accessed in blocks which are read or written in both directions.							
1.1.1 A Computer Peripheral							
DECTape is a peripheral for the "R" Family of Computers. Each DECTape system consists of a controller and from one to eight tape drives. The controller connects to the computer's I/O bus and communicates to the processor for control and status information; and directly to memory for data information. Each drive connects to the controller through a parallel bus through which both control and data information pass.							
There are two controller models and two models of tape drives. Table 1-1 lists these models, and the computer systems on which they are used. Note that the TC08 and TC08-N are functionally identical. Any significant differences will be indicated in the text.							
Table 1-1 DECTape Model Numbers							
Controller Model		Tape Drive Model		Computer System			
TC08		TU55, TU56		PDP8/L, PDP-8/E			
TC08-N		TU55, TU56		PDP8/L, PDP-8			
SIZE	A	CODE		NUMBER		REV	

ENGINEERING SPECIFICATION				CONTINUATION SHEET			
TITLE TC08 Specification							
1.6 Adjustment Procedures							
1.6.1 Delays and Clock							
1.6.2 Setting the Clock							
1.6.3 The Unit or Motion Delay							
1.7 Summary of Statistics							
SIZE	A	CODE		NUMBER		REV	

ENGINEERING SPECIFICATION				CONTINUATION SHEET			
TITLE TC08 Specification							
1.1.2 Stores Digital Data on 3/4 Inch Magnetic Tape							
Each transport contains motor, tape heads, and the logic necessary for selection, motion control and data transfer. Each drive can handle 260 foot reels of 3/4 inch 1 mil magnetic tape. Bits are recorded at a density of 350 ± 55 bits per track inch. The tape moves at a speed of 93 ± 12 inches per second, and can store up to 190,000 12-bit words. The TU55 has one drive, and the TU56 has two drives.							
1.1.3 Stores Data in a Three Track Serial/Parallel Format							
The data in the DECTape system is stored in a parallel format, in that each 12-bit data word is divided into 4 3-bit bytes, and stored in parallel across three data tracks. The system stores the complete 12-bit word serially along the tape in four of these bytes.							
1.1.4 Data Can Be Accessed in Blocks							
DECTape stores its data words in blocks or groups. Each block can be randomly accessed in that it is identified by a block number or address, and the controller under the direction of the computer can select at random any block to write or read a group of words.							
SIZE	A	CODE		NUMBER		REV	

TITLE TC08 Specification

The length, or number of words in each block is pre-determined when the tape itself is formatted. Formatting involves writing a timing track and a mark track on two (non-data) tracks of the tape, and numbering the data blocks. During formatting, the programmer can select the length of the blocks. Once set, the length cannot be changed without destroying data on the tape.

1.1.5 Data Can Be Accessed In Both Directions

Each block can be identified by the computer no matter which way the tape is moving. Further, data can be read or written in either direction. This feature allows the programmer relatively fast search time since the tape does not have to be re-wound before a block can be searched out, and the programmer can begin to write no matter which end of the block appears first. It is important, however, that the programmer read and write the same data in the same direction, or else be prepared to unscramble it in the computer.

1.2 Operational Description of DECTape

Information flow within the DECTape system is determined by the recording format on the tape surface, and the internal architecture of the controller.

SIZE	CODE	NUMBER	REV
A	00	TC08	

TITLE TC08 Specification

The two tracks next to the timing tracks are called mark tracks. These record the instructions which tell the TC08 controller where the tape is and what type of data is stored in the associated information tracks. The information or data tracks are placed in the middle of the tape, where the effect of skew is at a minimum. As are the timing and mark tracks, the data tracks are paired up.

The high reliability of the recording/reading system is because of the way in which the 10 tracks are divided into five pairs of counterparts. That is, corresponding heads for each track are wired in series, and record and write the same information. During reading, the analog sum of the two heads is used to detect the correct value of the bit. Therefore, a bit cannot be misread until the noise on the tape is sufficient to change the polarity of the sum of the signals being read. During writing, corresponding heads record the same information.

In summary, the five pairs of tracks consist of - the timing tracks used to strobe the other tracks, the mark tracks which store instructions, and three data tracks. An 12 bit PDP-8 word, then, used 4 lines of 3 data bits each.

SIZE	CODE	NUMBER	REV
A	00	TC08	

TITLE TC08 Specification

1.2.1 The Tape Surface Recording Format

Two important DECTape features - individually addressable blocks and bidirectional reading and writing, are the result of the tape surface format. This stores not only data, but also instructions telling DECTape what to do with the data.

1.2.1.1 DECTape Heads and Tape Tracks

Both the data and the instructions are stored in, or read from, the magnetic tape through read/write heads which magnetize the tape in one of two directions to represent a "0" or a "1", and read the same information back. There are ten read/write heads distributed along the width of the tape, each head covering a narrow path called a tape track or channel. Figure 1-1 shows a tape stretched over the ten heads to indicate how the width is divided into ten tracks.

The ten tracks and heads are divided functionally into five pairs. The two outside tracks are called timing tracks. On these tracks signals are pre-recorded at a fixed frequency, and used to strobe information into or from the other tracks. The tape controller synchronizes on these pulses.

SIZE	CODE	NUMBER	REV
A	00	TC08	

TITLE TC08 Specification

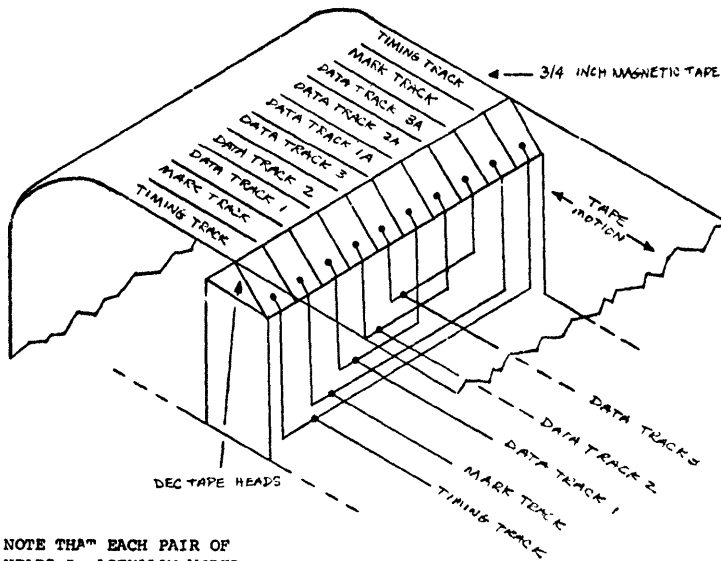
1.2.1.2 Tape Recording Format

A reel of tape must be pre-formatted before it can be used on the DECTape system. This involves logically dividing the 260 foot length into three zones - two end zones and a recording zone. The end zones are about 11 feet long and are used to wind tape around the heads and into the take-up reel. They never contain any data. The recording zone contains the data.

The recording zone is divided into blocks. Each block will store a specific number of data words and several control words, including its own address or block number. The number of words such a data block will store is determined when the tape is formatted. Normally, one reel is formatted with 1474 blocks, each with 129 12-bit words. However, the total length of the tape is equivalent to 884,736 lines which can be divided into any number of blocks up to 4,096. Complete instructions on how to format a tape are available in the DECTape Formatter. (The number of blocks is limited by this formatter).

SIZE	CODE	NUMBER	REV
A	00	TC08	

TITLE TC08 Specification



NOTE THAT EACH PAIR OF HEADS IS ACTUALLY WIRED IN SERIES, AND TWO WIRES ARE RUN TO A DIFFERENTIAL AMPLIFIER, FOR SIMPLICITY A SINGLE WIRE FOR EACH PAIR IS SHOWN HERE.

Figure 1-1 DECTape Heads and Tape Tracks

SIZE	CODE	NUMBER	REV
A	1	TC08 0 23	

TITLE TC08 Specification

Each data block on the tape has the following characteristics: (fig. 1-2)

1. It is numbered and its number is contained in the data tracks of the block number area at either end of the block. This is to say that the computer can identify a block from its number by approaching the block from either direction. The block can then be read or written into, in either direction.
2. A longitudinal parity checksum is automatically calculated by the controller and deposited into the parity check area of the block. There is a parity check at either end of the block so that the checksum can then be deposited no matter in which direction data has been read or written. When the data is read back, this checksum is re-calculated and compared with the original. Any discrepancy is reported to the computer.
3. Spaces are established to delineate blocks, and within each block, between the block number and the data area, so as to give the computer time to react to the number (i.e. set up the data parameters). The controller

SIZE	CODE	NUMBER	REV
A	1	TC08 0 23	

TITLE TC08 Specification

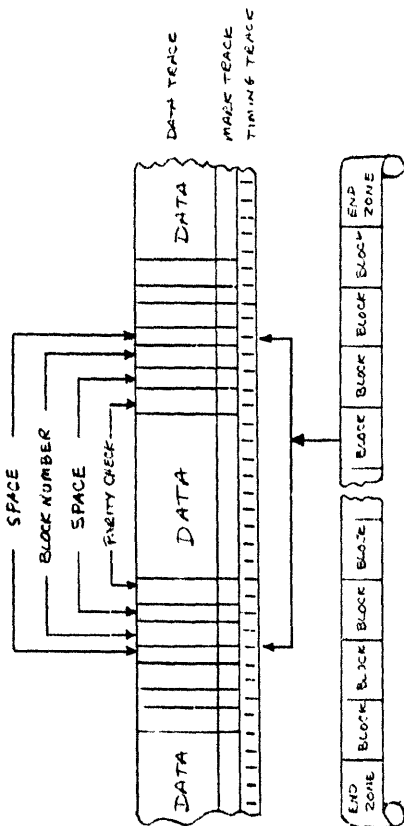


Figure 1-2 DECTape Recording Format

Showing the three zones and a Data Block Expanded to Illustrate Data and Control Areas

SIZE	CODE	NUMBER	REV
A	5	TC08 0 23	

TITLE TC08 Specification

identifies the different areas of a block, as well as the different zones on the tape, from special codes pre-recorded on the mark track. These codes are not seen by the computer, and are of no interest to the programmer except for the function that they perform. A more detailed breakdown of the mark track is given in Chapter 2.

1.2.2 The DECTape Architecture

The organization of the hardware in the controller is studied in three parts - the control, the data transfer section, and the formatter. These are shown in figures 1-3, 1-4, and 1-5.

1.2.2.1 The Control Section

The control section is that logic which comes under the supervision of the program through IOT instruction. (Table 1-2 describes the IOT instructions.) It consists of 7 registers and their associated logic. (Table 1-3 summarizes the decoding for each register.) Descriptions of the registers are as follows.

1. The Unit Select Register. A 3-bit register which feeds a binary to octal decoder, which in turn drives eight select lines to the control cable. Each transport can be dialed into a

SIZE	CODE	NUMBER	REV
A	1	TC08 0 23	

TITLE TC08 Specification

particular selection address by means of a switch on the front of the transport. If the number decoded from the Unit Select Register corresponds to the number selected on the switch then that transport will accept motion commands from the controller. If more than one transport is on the same number, then an error flag is posted as soon as an attempt is made to initiate operation.

2. The Motion Register. A 2-bit double buffered register that commands the selected transport to stop, go and move forward or go and move in reverse. Note that each transport remembers its motion, and if it is subsequently unselected without being stopped, it will continue until it is re-selected and stopped, or until it runs out of tape.

3. The Mode Register. This selects either continuous or normal mode for each operation of the function register. The difference in response for each function to the two modes is explained in Table 1-4.

4. The Function Register. This is 3-bits long, and is decoded by a binary to octal converter to select one of a possible seven functions. An explanation of these functions is given in Table 1-4.

SIZE	CODE	NUMBER	REV
A		TC08 0003	

TITLE TC08 Specification

All of these bits 0 to 9 can be read back into the computer under the instruction Read Status A. (DTRA).

The error flags can also be read into the accumulator into AC bits which correspond to the bits shown in Figure 1-3. Further, the DECTape flag is read into accumulator bit 11. Bits 0-6 and bit 11 are known collectively as Status B. The IOT instruction which reads them is called DTRB.

In Summary, the Status A registers are set under IOT command. They determine the operation to be performed, the transport which is to perform that operation, the direction of motion, and the mode. Any errors are communicated to the computer through the interrupt logic. If an operation is successful, then that too is communicated back to the computer, which then takes further action. The actual information transfers are taken care of through the multi cycle data break facility under the direction of the data transfer logic.

SIZE	CODE	NUMBER	REV
A		TC08 0003	

TITLE TC08 Specification

5. Enable the Interrupt. A 1-bit register which, when set, allows the controller to use its PI interrupt system. When reset, it disconnects DECTape from the interrupt lines. In the disconnect state none of the error conditions or DECTape flag can cause an interrupt. In no other way, however, is status B affected.

6. The ERROR Flags are flip flops which continually examine possible error conditions during the operation of the transport. Each condition is explained in Table 1-5.

7. The DECTape flag is also a single flip flop which sets, either when an operation has been successfully completed, or when it has been aborted as the result of an error.

The unit Select, Motion, Mode, Function and Enable registers are all set from the accumulator by the XOR status A IOT. The bits of Figure 1-5 indicate the accumulator bit which sets each flip flop. The two bits not shown, bit 10 and 11, clear the error flags and the DECTape flag respectively, if they are set to a zero in the AC during an XOR instruction. The complete word from 1 to 11 is known as Status A.

SIZE	CODE	NUMBER	REV
A		TC08 0003	

TITLE TC08 Specification

Table 1 - 2

Mnemonic	Octal Code	Description
DTCA	6762	Clear status register A. The DECTape control and error flags are undisturbed (D.F and I).
DTRA	6761	Read status register A. The content of status register A is ORed into the accumulator.
DTXA	6764	XOR status register A. The exclusive OR of the content of bits 0 through 9 of the accumulator and status A is loaded into status register A, and bits 10 and 11 of the accumulator are sampled to control clearing of the error and DECTape flags, respectively. The WC overflow flag is cleared.
DTLA	6766	Load status register A. Combines action of DTCA and DTXA to load AC0-9 into status register A. Bits 10 and 11 control clearing of error and DECTape flags, respectively.
DTLB	5774	The 3 memory field bits are loaded from AC bits 6-8. The AC is cleared and the error flags are left undisturbed.
DTRB	6772	Read Status B. The AC is cleared and the content of status B is ORed into the accumulator.
DTDF	6771	Skip on DECTape flag. The state of the DECTape flag (DTF) is sampled. If it is set to a 1, the content of the PC is incremented by one to skip the next sequential instruction.

SIZE	CODE	NUMBER	REV
A		TC08 0003	

TITLE TC08 Specification

TABLE 1-3 Status A-bit Assignments

Register	AC Bit	Register Bit	Octal Code	Decoding
Unit Select (USR)	0-2	0-2	000	Unit 0 or 8
			001	1
			010	2
			011	3
			100	4
			101	5
			110	6
			111	7
Motion (MR)	3	0	0 =	Forward (FWD)
			1 =	Reverse (REV)
	4	1	0 =	Stop motion (STOP)
			1 =	Start motion (GO)
Mode	5	0	0 =	Normal Mode (NM)
			1 =	Continuous mode (CM)
Function (FR)	6,7,8	0,1,2	000	Move
			001	Search
			010	Read Data
			011	Read all
			100	Write data
			101	Write all
			110	Write timing
			111	Unused (causes select error)
Enable the Interrupt (ENI)	9	0	1 =	Enable DECTape control flag (DTCF) to the program interrupt.
Error flag (EF)	10		0 =	Clear all error flags
			1 =	Error flags undisturbed
DECTape flag (DTP)	11		0 =	Clear DECTape flag
			1 =	DECTape flag undisturbed

SIZE A CODE SP NUMBER TC08-023 REV

TITLE TC08 Specification

Table 1 - 4

FUNCTION	OPERATION
SEARCH (Continued)	<p>This search operation is most efficient when both modes are used in the following way:</p> <ol style="list-style-type: none"> 1. The current block number is detected in normal mode. 2. The difference between it and the desired block number is computed, and the direction corrected, if necessary. 3. If the direction is reversed, read the current block again and compute the new difference, otherwise go to 4. 4. The two's complement of the difference is loaded into the word count register. 5. The function is changed to continuous mode. 6. On the next interrupt, the transport is over the desired block. The block number is in the address specified by the current address register.
READ DATA	<p>READ DATA is used to transfer blocks of data into core memory. The standard block length is 129 12-bit words. For this and all following functions, the CA location initially must be set to (the transfer memory location - 1) because the CA location is incremented just before each word transfer. The WC location is also incremented prior to each word transfer, so must be set to the 2's complement of the number of words to be</p>

SIZE A CODE SP NUMBER TC08-023 REV

TITLE TC08 Specification

Table 1 - 4 The DECTape functions

FUNCTION	OPERATION
MOVE	<p>The move function is used to re-wind tape. Code 000 of bits 6, 7, and 8 initiates tape motion in the selected direction, provided 40 is also on. The mark track is read, but only the end of tape instruction is decoded, and of tape posts an error flag and causes an interrupt to the computer. If the tape control is unselected but not stopped, it continues to run; however, the end of tape is not detected. The state of mode is irrelevant.</p>
SEARCH	<p>The search function is used to search for blocks. When a block number is detected by the mark track, the three-cycle data break control transfers the number into the address specified by the current address register. The current address register is not incremented, so that successive block numbers always go to the same address. The word count register is incremented, however, as each block number is passed. If the mode is set to normal, the DECTape flag is set each time a block number is detected. This causes an interrupt and the program can identify the block number. In continuous mode, no interrupt occurs until the word count register overflows.</p>

SIZE A CODE SP NUMBER TC08-023 REV

TITLE TC08 Specification

Table 1-4

FUNCTION	OPERATION
READ DATA (continued)	<p>transferred prior to the transfer. Data may be transferred in forward or reverse. Any number of words equal to or less than a block may be transferred in NM. The DTF is raised and an interrupt occurs at the end of each block. The DTF must be cleared before the beginning of the next block (i.e. 17 msec.) to avoid an erroneous timing error. When partial blocks are transferred data transmission will end with WC overflow (i.e. the word which causes the WC overflow is the last one transferred.) However, the remainder of the block is read and parity checked before the DTI and interrupt occur. Tape motion continues until the GO bit is reset to 0 by the program. If the GO bit is not reset to a 0 or a new function specified before the end of the next block, a timing error will occur. READ DATA in NM is intended primarily for single, 129-word block transfers. If any other number of words is to be transferred, it is advantageous to use CM. However, if the programmer chooses to use NM for any other number of words, the program must check for WC overflow at each interrupt because there is no other way to determine when to stop the tape or change to another function.</p>

SIZE A CODE SP NUMBER TC08-023 REV

ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE TC08 Specification			
Table 1 - 4			
FUNCTION	OPERATION		
READ DATA (continued)	When the WC overflow occurs, it is essential that the function be changed or the GO bit set to 0. Otherwise transfer begins again (the IOT to clear the DTF implicitly specifies the same function again) at the next block (or next word for the ALL functions) since WC-00008 is valid. Any number of words may be transferred in CM. However, the DTF and an interrupt occur only once after a WC overflow and an end of block. The comments concerning tape continuation apply in CM as well as NM.		
READ ALL	<p>The READ ALL function allows information to be read from unusually formatted tape; essentially reading all data tracks recorded on DECTape regardless of the mark track value. During the READ ALL function the DECTape control does not distinguish between different marks recorded on the mark track - except to check for mark track errors (MTRK).</p> <p>In normal mode (NM) the DTF is raised and causes an interrupt at the end of each 12-bit word transfer. Data transfer stops after WC overflow, but tape motion continues until GO bit is set to 0 or a new function is specified (in both NM and CM). If the DTF is not cleared after each word transfer, a timing error occurs at the end of the next word (i.e. 33 microseconds later).</p>		
SIZE	CODE	NUMBER	REV
A	SP	TC08-0-23	

DEC FORM NO 16-1022
DRA 108

SHEET 21 OF 50

ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE TC08 Specification			
Table 1 - 4			
FUNCTION	OPERATION		
WRITE DATA (continued)	In continuous mode, the DTF is set at the end of the block in which WC overflow occurred. Thereafter, if no new function is specified, the tape continues to move but the writers are disabled, and an error will occur.		
WRITE ALL	<p>All the details of the READ ALL function description apply. The WRITE ALL function is used to write an unusual format (such as block numbers on DECTape after timing and mark tracks have been recorded). The word which causes WC to overflow is the last one written in NM or CM. The tape continues to move but the writers are disabled.</p> <p>NOTE: Change of function must be delayed for 90 microseconds to insure recording of last word. Alternative method: set WC to one greater than desired number of word transfers and change function within 40 microseconds after WC overflow.</p> <p>NOTE: The WC is in location 7750 The CA is in location 7751</p>		
SIZE	CODE	NUMBER	REV
A	SP	TC08-0-23	

DEC FORM NO 16-1022
DRA 108

SHEET 22 OF 50

ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE TC08 Specification			
Table 1-4			
Function	Operation		
READ ALL (Continued)	For continuous mode, the DTF is raised and causes an interrupt at WC overflow only. If this interrupt is ignored no more data transfers occur but tape motion continues to EOT.		
WRITE DATA	<p>The write enable switch on the TU55 or TU56 must be in write enable position for all WRITE functions. All the details of the READ DATA function description apply with the following exceptions.</p> <p>In normal mode, the DTF is set to 1 at the end of each block. If WC overflow did not occur in the block just ended and a new function is specified, the next block will be processed provided the DTF has been cleared. If WC overflow did occur in the block just ended and no new function is specified, the tape continues to move but the writers are disabled, and an error will occur. The remainder of the block is written with zeroes.</p> <p>In both CM and NM when partial blocks are written, data transfer from core to DECTape stops at WC overflow. All zeroes are written in the remaining data words of the block and the parity check character is computed over the entire block and recorded.</p>		
SIZE	CODE	NUMBER	REV
A	SP	TC08-0-23	

DEC FORM NO 16-1022
DRA 108

SHEET 23 OF 50

ENGINEERING SPECIFICATION		CONTINUATION SHEET	
TITLE TC08 Specification			
Table 1-5 The Error Flags			
FLAG			
ERROR FLAG	<p>Five types of errors can be detected in the use of DECTape:</p> <ul style="list-style-type: none"> Timing Error Parity Error Select Error End of Tape Mark Track Error <p>For all errors the EF is raised, a bit is set in the status register and an interrupt occurs (if the enable-to-interrupt bit has been set). The DTSP instruction skips on the inclusive OR of those error bits; hence, each status bit must be checked to determine the kind of error. For all but the parity error, the selected transport is stopped and the EF is raised at the time of the error detection. No DTF occurs. For a parity error, the GO bit remains 1 (i.e., motion continues) and the EF is raised simultaneously with the DTF in NM. Only 1 interrupt occurs; hence the program must check the EF.</p> <p>A parity error in CM raises the EF at the end of the block in which the parity error occurs causing an interrupt (if enabled). If no program action is taken, e.g. stop transport or reverse and re-read, data transfer continues and the DTF is raised and causes an interrupt at WC overflow and end of final block read.</p>		
SIZE	CODE	NUMBER	REV
A	SP	TC08-0-23	

DEC FORM NO 16-1022
DRA 108

SHEET 24 OF 50

TITLE TC08 Specification

Table 1 - 5

FLAG	
MARK TRACK ERROR BIT 1	A mark track error occurs if the DECTape control fails to recognize a legitimate mark on the mark track. The error may occur in all but the move or write timing and mark track functions. In both CM, and NM, the LF is raised, the tape transport stops and an interrupt occurs.
END OF TAPE ERROR BIT 2	An EOT error occurs when the DECTape enters either end zone with the GO bit = 1 and the forward/reverse direction bit set to continue in the same direction. In NM and CM data transfer stops at the last legitimate block, the LF is raised, the tape transport stops and an error interrupt occurs.
SELECT ERROR BIT 3	Select Error * - A select error will result under any of the following conditions: <ol style="list-style-type: none"> 1. Selection of none or more than 1 transport. 2. Attempt to write on DECTape transport with WRITE ENABLE/WRITE LOCK switch in the WRITE LOCK position. 3. Attempt to select unit for any function with DECTape transport REMOTE/OFF/LOCAL switch in the OFF or LOCAL (off-line) position. 4. Attempt to write timing and mark tracks with the DECTape control switch in any position other than write timing and mark

SIZE	CODE	NUMBER	REV
A	SP	TC08-0-23	

TITLE TC08 Specification

1.2.2.2 The Data Transfer Section

The data transfer section (Figure 1-4) handles the flow of information between the multi cycle data channel of the computer, and the magnetic read/write heads. There are two types of information - data, and instructions from the tape which tell the controller what to do with the data. The instructions are recorded on the mark track, which feeds the window register and subsequently the data control logic. This combination looks at the mark track codes and from them determines whether the tape heads are over end zones or recording zones; and if over recording zones, where in any particular block. Meanwhile, data from the three data heads, and timing pulses from the timing track heads are feeding the data buffer and the data control logic respectively. The timing pulses are used to strobe the mark track and data track information at the proper time. Data comes into the controller in bytes of three, therefore the data buffer is basically two 6-bit shift registers.

As the data is shifted in, the longitudinal parity buffer calculates the parity of each track. When a complete block has been read, this buffer should be all ones if no error has been detected. If it is not all ones, then a parity error flag

SIZE	CODE	NUMBER	REV
A	SP	TC08-0-23	

TITLE TC08 Specification

Table 1-5

FLAG	
SELECT ERROR (continued)	track. 5. Attempt to perform any function other than write timing and mark tracks with the DECTape control switch in the write timing and mark track position. 6. Attempt to execute unused function (Octal code 7). *No-tape or tape-run-off-reel conditions are not detectable.
PARITY ERROR	Parity Error - A parity error occurs only during the READ DATA function for a hardware computed parity check character (PCC) failure.
TIMING ERROR	Timing Error - A timing error (program malfunction) is a data miss or program failure to clear the DTF status bit. A timing error occurs also if the program switches to READ or WRITE DATA function while the DECTape is currently passing over a data area on tape.

SIZE	CODE	NUMBER	REV
A	SP	TC08-0-23	

TITLE TC08 Specification

is raised.

During a Read operation the data buffer accumulates a complete 12-bit word, and transfers it to the DECTape buffer for temporary storage. The Data Channel flag is then raised and a multi cycle data channel break initiated. During the break, this word is transferred out of the DECTape buffer into the location specified by the current address register at location 7750. The word count at location 7751 is incremented. The computer is allowed a maximum of 33 us. to complete this operation.

If the computer has not responded in time, an error flag is raised to show the timing error.

Alternately, if a write operation is required, the TC08 requests a multi cycle data channel break. The computer transfers the word to be written into the DECTape buffer, which is then transferred into the Data Buffer at the right time. From the data buffer it is shifted out and written onto the tape. Meanwhile, the TC08 requests another word from the computer as soon as the DECTape buffer is emptied into the Data Buffer, and the TC08 is ready to write the next piece of data.

SIZE	CODE	NUMBER	REV
A	SP	TC08-0-23	

TITLE TC08 Specification

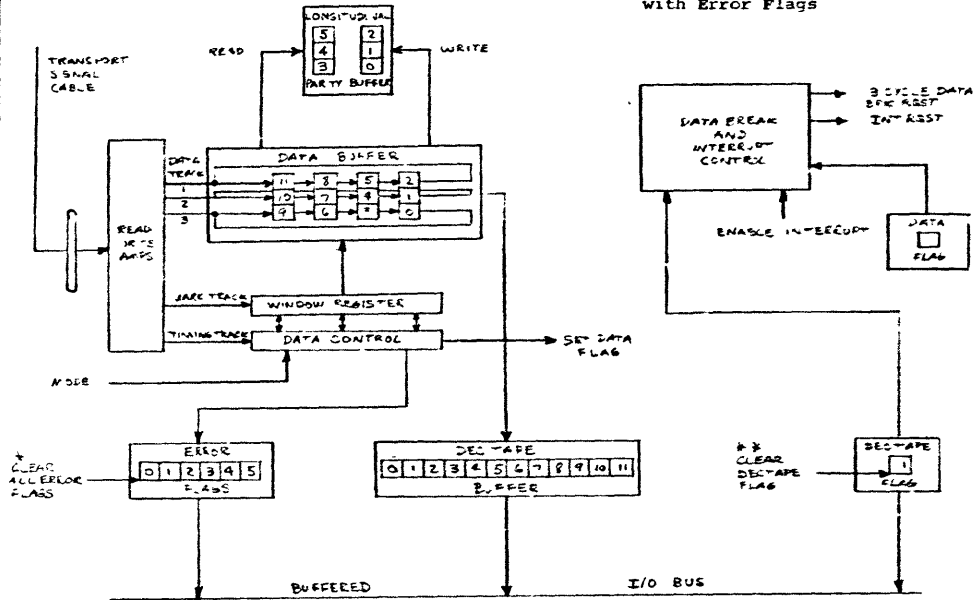
At the end of a transfer, the word count overflows, and the DECTAPE flag is raised. When a PLIC location is initiated, as explained in Table 1-4.

1.2.2.3 The Formatter Section

Before a reel of DECTAPE can be used in a system, it must first be formatted. This involves writing the proper mark track codes, numbering the data blocks, and writing in the timing track. A program called the DECTAPE Formatter is available for doing this. The program specifies the Write Timing and Mark Track function and transfers the correct mark track code through the data channel into the DECTAPE buffer, as shown in figure 1-5. Only bits 0, 3, 6 and 9 are used. The controller switch must be on WRTM. These bits are loaded into the proper shift register of the Data Buffer, which then shifts them into the mark track write head and so to the tape. In normal mode the DECTAPE flag is raised after each word is transferred to the mark track. In continuous mode, the DECTAPE flag is raised when the Word Count overflows. Meanwhile, the timing track writer is recording a clock pulsed on the timing track.

TITLE TC08 Specification

Figure 1-3 Data Transfer Section with Error Flags



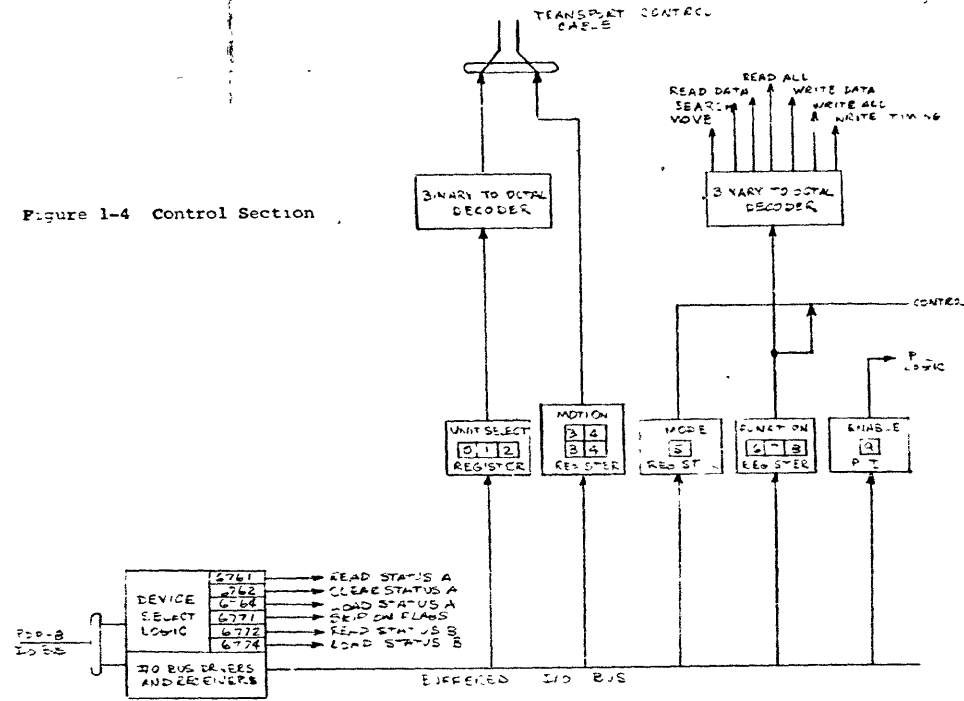
- NOTES:
- * This pulse is generated by AC bit 10 in a Zero "ANDED" with the IOP Pulse from the IOT instruction.
 - ** This Pulse is generated with AC Bit 11 is on a Zero during the IOT instruction.

TITLE TC08 Specification

The block numbers are written in WRITE ALL mode after the mark and timing tracks have been written.

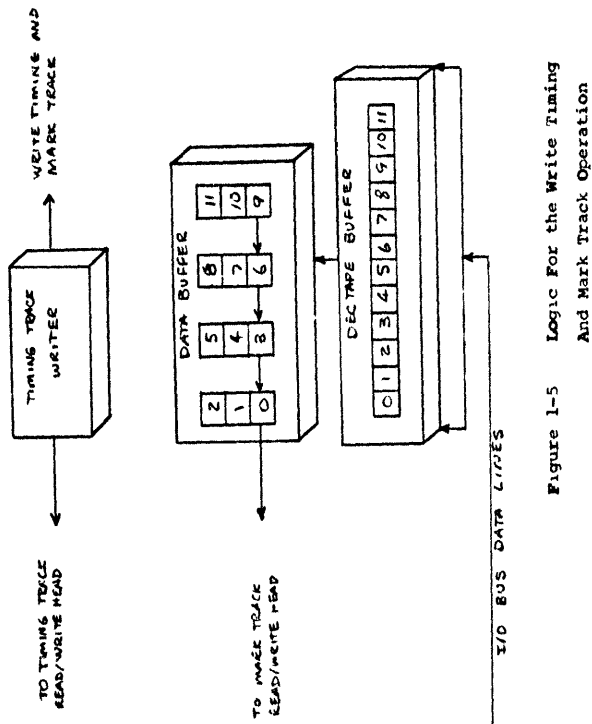
TITLE TC08 Specification

Figure 1-4 Control Section



TITLE TC08 Specification

TITLE TC08 Specification



SIZE	CODE	NUMBER	REV
A	S?	TC08-0-23	

TITLE TC08 Specification

Table 1 - 6

INDICATOR NAME	INDICATOR FUNCTION
TIM	This flag indicates timing errors.
DTF	This lamp reflects the state of the DECTape flag. (ON indicates an operation completed).
DF	The Data Flag is set when the controller needs to transfer a data word through the three-cycle break.
WC	The Word Count flag is zeroed whenever the word count register overflows.
U+M	This is the output of the up to speed delay. When the light is on it indicates that the tape is not yet up to speed.

SIZE	CODE	NUMBER	REV
A	S?	TC08-0-23	

TITLE TC08 Specification

1.3 TC08 Operator Controls and Indicators

The single switch, WRPM/NORMAL, and an array of lights are all with which the operator of the TC08 controller need concern himself. The operation of the transports is explained in their respective manuals. The TC08 switch (located on the left-hand side of the logic panel) puts the controller in write timing and mark track mode or else in normal, or every other mode, depending on the settings, SWPM or NORMAL respectively. Table 1 - 6 summarizes the function of each indicator.

Table 1 - 6 The Indicator Panel

INDICATOR NAME	INDICATOR FUNCTION
USR	The Unit Select Register which specifies which transport is to be activated.
MR	The Motion Register specifies the three possible movements of the reel.
FR	This four-bit Function Register specifies one of several possible operations in either of two modes.
ENI	Enable the interrupt when on indicates that the controller can cause a program interrupt when an error flag or the DECTape flag is set.

SIZE	CODE	NUMBER	REV
A	S?	TC08-0-23	

TITLE TC08 Specification

Table 1 - 6

INDICATOR NAME	INDICATOR FUNCTION
EF	This flag is set if any one of the five following error flags come up. These conditions stop transport motion, except for the parity error of bit 4, and all cause a program interrupt if the facility is enabled.
MK	The output from the mark track instruction register is tested every time an instruction appears. If no instruction appears, this indicates that the mark track is not recorded properly and therefore an error has occurred. MK and therefore EF are set.
END	If the instruction register of the mark track decodes an end zone indicator, this flag and EF are set. A subsequent program interrupt stimulates the computer to determine the cause of the interrupt.
SE	This flag indicates select errors when control switch states and Status A function states are compared and found incongruous.
IPAR	This error occurs if the longitudinal parity buffer shows an error at the end of a block during a read data function.

SIZE	CODE	NUMBER	REV
A	S?	TC08-0-23	

TITLE TC08 Specification

Table 1 - 6

INDICATOR NAME	INDICATOR FUNCTION
UTS	This Up-to-Speed flip-flop is set as soon as the tape transport reaches an acceptable speed.
W	This flag, when set, indicates that the writers are enabled.
WTM	This means the SWTM/NORMAL switch is in write timing and mark track mode (SWTM).
LPB	These six indicators reflect the state of the Longitudinal Parity Buffer.
STATE	These bits make up the state generator, a ring counter, which steps from an idle state through five other states and back to idle, as a block passes the tape heads.

SIZE CODE NUMBER REV
A 01 TC08-0103

TITLE TC08 Specification

Table 1 - 6

INDICATOR NAME	INDICATOR FUNCTION
MC	These three bits represent a three-bit switched tail counter composed of bits MC00, MC01, MC02.
C0, C1	These are the flip-flops which constitute the counters of the timing generator.
DTB	These lights reflect the states of the 12-bit DECTape buffer.
WINDOW	The Window Register is a simple shift register which receives the instruction codes from the mark track and uses the codes to set the State Generator.

SIZE CODE NUMBER REV
A 01 TC08-0103

TITLE TC08 Specification

Table 1 - 6

INDICATOR NAME	INDICATOR FUNCTION
BM	Block Mark is the first bit to which the state generator moves. It is set when forward block mark is in the data buffer.
RC	The Reverse Checksum state occurs when the Reverse PCC Mark cell is encountered.
D	The Data State starts with the first block that contains data (The Reverse Final Mark) and finishes when the next-to-last data block (the Prefinal Mark) Passes the read heads.)
F	The Final State occurs during the last cell which contains data (the Final Mark.)
CK	The Checksum State occurs when the PCC Mark cell passes the heads. During this state, the checksum is deposited in the PCC Mark, if the TC08 is writing; it checks for a parity error, if the TC08 is in a read operation.
I	The idle state.

SIZE CODE NUMBER REV
A 01 TC08-0103

TITLE TC08 Specification

1.4 Programming Examples

The following is an example of programming the TC08. The program is written in PDP-8 Assembler languages.

Problem: Find a given block, number 5. The transport number is 3.

TAG	INSTRUCTION	REMARKS
SRCH,	Ø ION CIA	/Turn on PI
	TAD 3614 DTCA DTXA JMP I SRCH	/Status A code for search, etc /Clear Status A /Load Status A /Return
Ø	ØØØØ	
1,	JMP FLAG	
FLAG	DTSK JMP + 2 JMS TAPE HLT	/Skip on flag /Error, DECTape flag was not set. Another system flag caused the PI
TAPE,	CIA ØIRB DCA TEMP AND 0001 SZA HLT CIA TAD TEMP AND 1000 SZA JMP ERROR JMP BLKNO	/Read Status B /Store it away /Mask for flag /Flag is on /No flag - something wrong /Return Status B /Test for error flag /Go to error subroutine /Go to subroutine to get block

SIZE CODE NUMBER REV
A 01 TC08-0103

TITLE TC08 Specification

```

BLKNO,   CLA
          TAD I CA      /Get block number
          TAD 7773     /Test for block 5
          SNA
          JMS WRT      /This is block 5-start writin
          CLA          /Not block 5
          TAD 5        /Get a 5
          CIA          /Make 2's compliment of 5
          TAD I CA     /Add present block
          CIA          /2's compliment it
          DCA WC       /Put result in WC
          CLA
          TAD 0100     /Get next Status A
          DTXA        /X'OR into Status A, CM
          ION         /Turn PI
          JMP I SRCH   /Go back to main program
    
```

SIZE	CODE	NUMBER	REV
A	SP	TC08-0-23	

TITLE TC08 Specification

1.6 Adjustment Procedures

1.6.1 Delays and Clock

1.6.1.1 The posts on the G888 reader writers should not be adjusted. They are pre-set in Module Production.

1.6.1.2 Set the XSTA Dy to 5 us. This delay will be triggered by the following program:

ADDRESS	INSTRUCTION	DESCRIPTION
0000	7604	Load AC from SR
0001	6766	Load Status A
0002	5000	Jump to Zero

The output of the delay is on pin D18T2. Adjust the bottom pot of the M302 in D16 so that the output signal has a positive duration of 5 microseconds.

1.6.1.3 The Status A register can also be tested with this program. By placing the data switches to A "1", the corresponding Status A bits will be set to A "1".

1.6.1.4 To check tape motion, set switches 0, 1, and 2 to select a transport and 3 and 4 to determine direction and motion.

1.6.2 Setting the Clock

1.6.2.1 The M401 clock will be enabled by the following procedure. Do not attempt to ground any signals with jumps; or modules may be destroyed. Toggle in the following program.

SIZE	CODE	NUMBER	REV
A	SP	TC08-0-23	

TITLE TC08 Specification

1.5 Equipment Description

1.5.1 Hardware

The TC08 Consists of two mounting panels of M series logic, an indicator panel, and associated power supplies and controls. The logic and indicator panel are mounted in the same cabinet as the power supplies, the power control and tape transports according to the configurations described in the PDP-8 Installation Manual.

1.5.2 Environmental Requirements

The DECTape system is designed to operate in a temperature range from 65 F (18 C) to 90 F (35 C) at a relative humidity of 10% to 55% with no condensation. The air should be free of dust and corrosive pollutants.

1.5.3 Power Requirements

Table 1-7 lists the primary power requirements for a DECTape system.

Table 1-7 DECTape Power Requirements

Configuration (no. of Transports)	No. of Cabinets	AC		Dissipation	
		Current (Amps)	Heat BTU/HR (max)	Power (KW)	
TU56					
1	1	4	1,516.6	446	
2	1	7	2,706.6	796	
3	1	10	3,896.6	1,146	
4	2	13	5,086.6	1,496	

SIZE	CODE	NUMBER	REV
A	SP	TC08-0-23	

TITLE TC08 Specification

ADDRESS	INSTRUCTION	DESCRIPTION
0000	7604	Load AC from SR
0001	6762	Clear Status A
0002	6767	XOR Status A
0003	7700	Clear AC
0004	5002	Jump to 2

Remove the tape from the transport and place it on line write enable. Turn the switch WRTM/NORMAL to WRTM. Set the data switches 4, 5, 6 and 7 to a one (1); hit Load Address and start. A WRTM function will be executed on unit eight (8), and the clock will run.

The output of the clock is on pin D15D2. Adjust the pot on the M401 in D15 so that the pulse repetition rate at this pin is 8.33 microseconds.

1.6.3 The Unit or Motion Delay

1.6.3.1 Load the DECTape basic exerciser and run test zero (0) to make the tape rock.

1.6.3.2 The output of the U + M Dy is on pin D14K1. Adjust the top pot on the M307 in D14 so that a positive signal with a positive duration of 120 milliseconds appears on this pin.

1.6.4 The Rate Delay

1.6.4.1 The output of the SP Dy is on pin D14H2. Adjust the bottom pot on the M307 and D14 for a positive signal with a duration of 70 microseconds on this pin.

1.6.5 Cross Talk Delays

1.6.5.1 The output of TP0 XTJK Dy is at pin A14F2. Adjust the top pot of the M302 in slot A14 so that this pin gives a positive signal with a duration of 10 microseconds.

SIZE	CODE	NUMBER	REV
A	SP	TC08-0-23	

TITLE TC08 Specification

1.6.5.2 The TPL XTLK Dy output is at pin A14T2. Adjust the bottom pot of the M302 in location A14 so that this pin gives a positive signal with a duration of 10 microseconds.

1.7 Summary of Statistics

The following tables summarize the errors, functions, flags and critical timing specifications of a DECTape system.

Table 1-8 Summary of Errors

FUNCTION	ERROR (IN NORMAL OR CONTINUOUS MODE)
Move	Select Error EOT*
Search	Select Error EOT* Timing Error MK TRK Error
Read Data	Select Error EOT* Timing Error Parity Error MK TRK Error
Read All	Select Error EOT* Timing Error MK TRK Error
Write Data	Select Error EOT* Timing Error MK TRK Error

*End of Tape

SIZE CODE NUMBER REV
A 10 TC08 0-10

TITLE TC08 Specification

Table 1-9 Summary of Functions

FUNCTION	NORMAL MODE (NM)	CONTINUOUS MODE (CM)
0. Move	DTF: No Interrupt CA*: Ignored WC**: Ignored	Same as NM
1. Search	DTF: Interrupt at each block mark CA: No incremented WC: Incremented at each block mark	DTF: Interrupt at each block mark if WC has overflowed CA: Not incremented WA: Incremented at each block mark
2. Read Data	DTF: Interrupt at end of each block CA: Incremented at each word transfer WC: Incremented at each word transfer	DTF: Interrupt at end of block if WC has overflowed. CA: Incremented at each word transfer WC: Incremented at each word transfer.
3. Read All	DTF: Interrupt at each word transfer CA: Incremented at each word transfer	DTF: Interrupt at WC overflow CA: Incremented at each word transfer.

SIZE CODE NUMBER REV
A 10 TC08 0-10

TITLE TC08 Specification

Table 1-8

FUNCTION	ERROR (IN NORMAL OR CONTINUOUS MODE)
Write All	Select Error EOT* Timing Error MK TRK Error
Write Timing & Mark Tracks	Select Error Timing Error

*End of tape

SIZE CODE NUMBER REV
A 10 TC08 0-10

TITLE TC08 Specification

Table 1-9

FUNCTION	NORMAL MODE (NM)	CONTINUOUS MODE (CM)
	WC: Incremented at each word transfer	WC: Incremented at each word transfer
4. Write Data	Same as 2.	Same as Read Data
5. Write All	Same as 3.	Same as Read All
6. Write Timing & Mark Tracks	Same as 3.	Same as Read All
7. Unused***		

*Current Address (CA) is in location 77^1
**Word Count (WC) is in location 77^0
***If used by mistake, the control gives a Select Error (SE)

SIZE CODE NUMBER REV
A 10 TC08 0-10

TITLE TC08 Specification

Table 1 - 10 Summary of Timing

OPERATION	TIME
Time to answer data channel request	Up to 33 microseconds
Word Transfer Rate	1 12-bit word every 133 microseconds
Block Transfer Rate	1 129 Block every 25 milliseconds
Start Time	375 milliseconds ($\pm 20\%$)
Stop Time	375 milliseconds ($\pm 20\%$)
Turn Around Time	375 milliseconds ($\pm 20\%$)
Search - Read Data Function change for present block	Up to 400 microseconds
Search - Write Data Function change for present block	Up to 400 microseconds
Read - Search Function change for next block number	Up to 1000 microseconds
Write - Search Function change for next block number	Up to 1000 microseconds

SIZE	CODE	NUMBER	REV
A	SP	TC08-003	

SHEET 49 OF 50

TITLE TC08 Specification

Table 1-10

OPERATION	TIME
DTF to beginning of next data block	1.7 milliseconds
DTF Occurrence:	
Move: NM, CM	Never
Search: NI	
Read Data: NM	Every 54 milliseconds
Write Data: NM	
Search: CM	(WC) X53 milliseconds
Read Data: CM	(No. of blocks)
Write Data: CM	X53 milliseconds
Read All: NM	
Write All: NM	Every 33 microseconds
Write Timing & Mark Tracks: NM	
Read All: CM	
Write All: CM	(WC) 33 microseconds
Write Timing & Mark Tracks: CM	

SIZE	CODE	NUMBER	REV
A	SP	TC08-003	

SHEET 50 OF 50

